


South Peak 15" Schematics

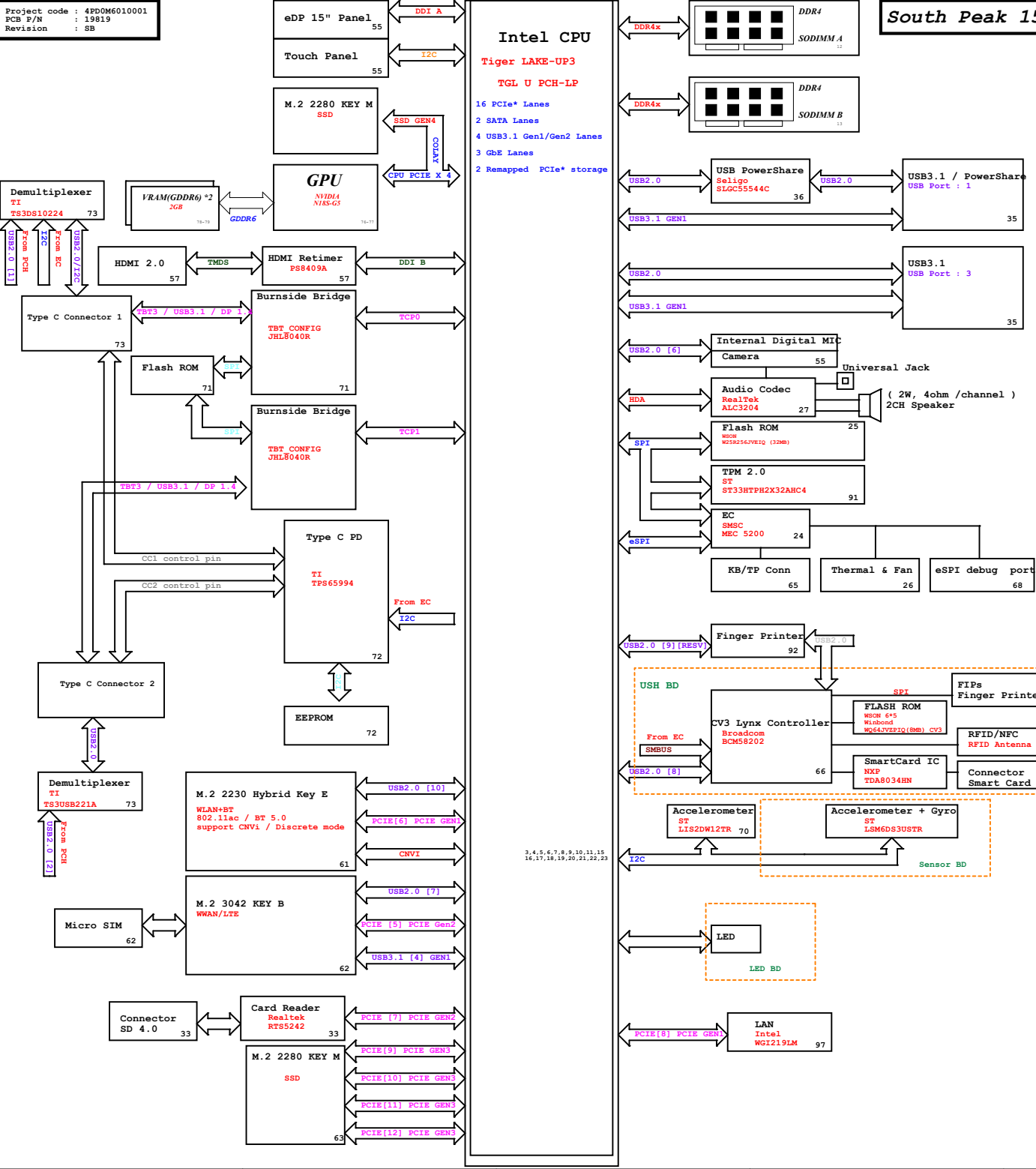
Tiger Lake-UP3

2020-04-24

REV: SB

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Cover Page			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 1 of	106



South Peak 15" Block Diagram

Main Func = CPU

eDP

eDP_TX_CPU_N0 <<< 55
eDP_TX_CPU_P0 <<< 55
eDP_TX_CPU_N1 <<< 55
eDP_TX_CPU_P1 <<< 55
eDP_TX_CPU_N2 <<< 55
eDP_TX_CPU_P2 <<< 55
eDP_TX_CPU_N3 <<< 55
eDP_TX_CPU_P3 <<< 55

55 eDP_AUX_CPU_N <<< 55
55 eDP_AUX_CPU_P <<< 55

EDP_HPDI >>> 55

eDP_BLEN_CPU <<< 55
eDP_BLCtrl_CPU <<< 55
eDP_VDDEN_CPU <<< 55

USB_OC1# >>> 35

DP to MUX

DP2_DDI_TX_N0 <<< 57
DP2_DDI_TX_P0 <<< 57
DP2_DDI_TX_N1 <<< 57
DP2_DDI_TX_P1 <<< 57
DP2_DDI_TX_N2 <<< 57
DP2_DDI_TX_P2 <<< 57
DP2_DDI_TX_N3 <<< 57
DP2_DDI_TX_P3 <<< 57

DP_HPDI_CPU <<< 57
57CPU_DP2_CTRL_CLK <<< 57
57CPU_DP2_CTRL_DATA <<< 57

KB_DET# <<< 65

TBT2_LSX0_RXD <<< 4,15,71

71 USB1_TCSS_RX_P1 <<< 71
71 USB1_TCSS_RX_N1 <<< 71
71 USB1_TCSS_RX_P0 <<< 71
71 USB1_TCSS_RX_N0 <<< 71
71 USB1_TCSS_TX_P1 <<< 71
71 USB1_TCSS_TX_N1 <<< 71
71 USB1_TCSS_TX_P0 <<< 71
71 USB1_TCSS_TX_N0 <<< 71
71 USB1_TCSS_AUX_P <<< 71
71 USB1_TCSS_AUX_N <<< 71

71 USB2_TCSS_RX_P1 <<< 71
71 USB2_TCSS_RX_N1 <<< 71
71 USB2_TCSS_RX_P0 <<< 71
71 USB2_TCSS_RX_N0 <<< 71
71 USB2_TCSS_TX_P1 <<< 71
71 USB2_TCSS_TX_N1 <<< 71
71 USB2_TCSS_TX_P0 <<< 71
71 USB2_TCSS_TX_N0 <<< 71
71 USB2_TCSS_AUX_P <<< 71
71 USB2_TCSS_AUX_N <<< 71

71 TBT_LSX0_TXD <<< 71
15,71TBT_LSX0_RXD <<< 71

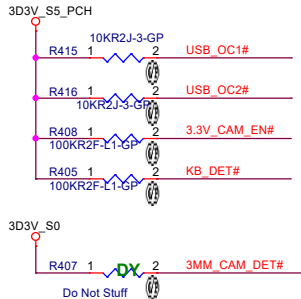
71 TBT2_LSX0_TXD <<< 71
4,15,71TBT2_LSX0_RXD <<< 71

3.3V_CAM_EN# <<< 40

HDMI 2.0

TBT

CY20 CPU_DISP_HPDI4



CPU1A

1 OF 21

eDP_TX_CPU_P3 AC2
eDP_TX_CPU_N3 AC1
eDP_TX_CPU_P2 AD2
eDP_TX_CPU_N2 AD1
eDP_TX_CPU_P1 AF1
eDP_TX_CPU_N1 AF2
eDP_TX_CPU_P0 AG2
eDP_TX_CPU_N0 AG1

eDP_AUX_CPU_P AJ2
eDP_AUX_CPU_N AJ1

DN4
DT6
GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
GPP_E23/DDPA_CTRLDATA

EDP_HPDI DR5
GPP_E14/DDSP_HPDI4/DISP_MISCA

DP2_DDI_TX_P3 T12
DP2_DDI_TX_N3 T11
DP2_DDI_TX_P0 Y9
DP2_DDI_TX_N0 Y9
DP2_DDI_TX_P1 T9
DP2_DDI_TX_N1 P9
DP2_DDI_TX_P2 V11
DP2_DDI_TX_N2 V9

AB9
AD9
DDIB_TXP3
DDIB_TXN3
DDIB_TXP2
DDIB_TXN2
DDIB_TXP1
DDIB_TXN1
DDIB_TXP0
DDIB_TXN0

DDIB_AUX_P
DDIB_AUX_N

CPU_DP2_CTRL_CLK DM29
CPU_DP2_CTRL_DATA DK27
GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
GPP_H17/DDPB_CTRLDATA

DP_HPDI_CPU DG43
GPP_A18/DDSP_HPDI4/DISP_MISCB/I2S4_RXD

3.3V_CAM_EN# DG47
KB_DET# DJ47
GPP_A21/DDPC_CTRLCLK/I2S5_TXD
GPP_A22/DDPC_CTRLDATA/I2S5_RXD

TBT_LSX0_TXD DU8
TBT_LSX0_RXD DV8
GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD

TBT2_LSX0_TXD DF6
TBT2_LSX0_RXD DD6
GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD

DN23
DM23
GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/DDP3_CTRLCLK/TBT_LSX2_RXD/GSPI2_CLK

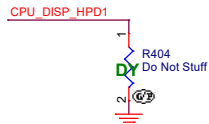
DK23
DN21
GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
GPP_D12/ISH_SPI_MOS/DDP4_CTRLCLK/TBT_LSX3_RXD/GSPI2_MOSI

3MM_CAM_DET# DF43
CPU_DISP_HPDI DF45
GPP_A17/DISP_MISCC/I2S4_TXD
GPP_A19/DDSP_HPDI1/DISP_MISCC/I2S5_SCLK
GPP_A20/DDSP_HPDI2/DISP_MISCC/I2S5_SFRM

USB_OC1# DH52
USB_OC2# DK45
GPP_A14/USB_OC1#/DDSP_HPDI3/I2S3_RXD/DISP_MISCC/DMIC_CLK_B1
GPP_A15/USB_OC2#/DDSP_HPDI4/DISP_MISCC/I2S4_SCLK

eDP_VDDEN_CPU DM8
eDP_BLEN_CPU DN8
eDP_BLCtrl_CPU DG10
EDP_VDDEN
EDP_BLCtrl
EDP_BLCtrl

TGL-U1-GP-U1
ZZ.00CPU.481



TCP0_TXRX_P1 AY2
TCP0_TXRX_N1 AY1
TCP0_TXRX_P0 BB1
TCP0_TXRX_N0 BB2
TCP0_TX_P1 AM5
TCP0_TX_N1 AM7
TCP0_TX_P0 A17
TCP0_TX_N0 A15
TCP0_AUX_P AP7
TCP0_AUX_N AP5

AT2
AT1
AT1
AU1
AU2
AD5
AD7
AH7
AH5
AF7
AF5

USB1_TCSS_RX_P1
USB1_TCSS_RX_N1
USB1_TCSS_RX_P0
USB1_TCSS_RX_N0
USB1_TCSS_TX_P1
USB1_TCSS_TX_N1
USB2_TCSS_RX_P1
USB2_TCSS_RX_N1
USB2_TCSS_TX_P0
USB2_TCSS_TX_N0
USB2_TCSS_AUX_P
USB2_TCSS_AUX_N

BF1
BF2
BE2
BE1
BD7
BD5
AY5
AY7
BB5
BB7

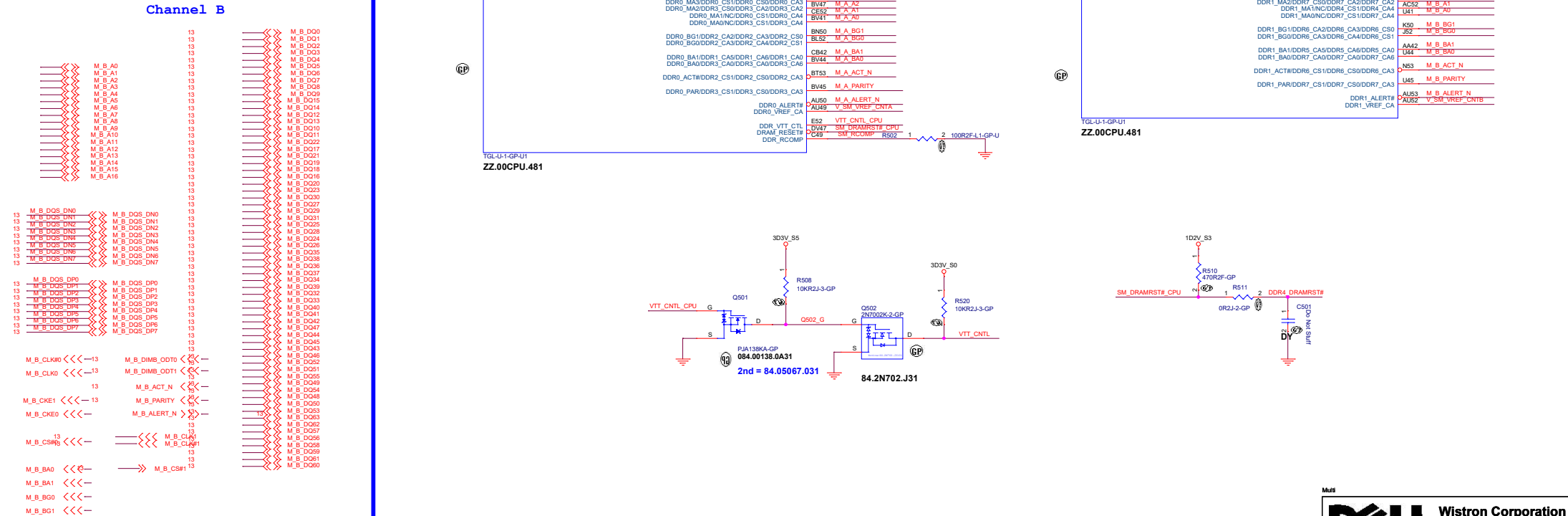
BK1
BK2
BJ2
BJ1
BM7
BM5
BH5
BH7
BK5
BK7

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX_N BK7

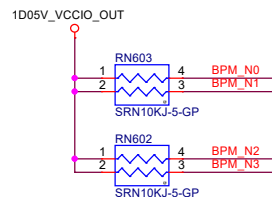
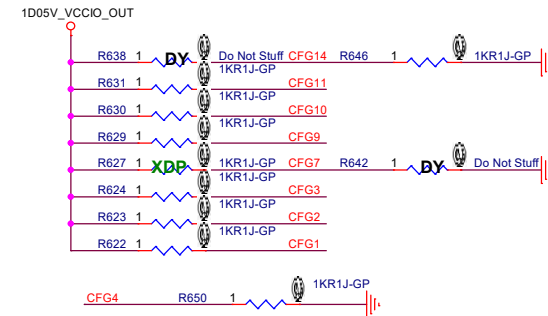
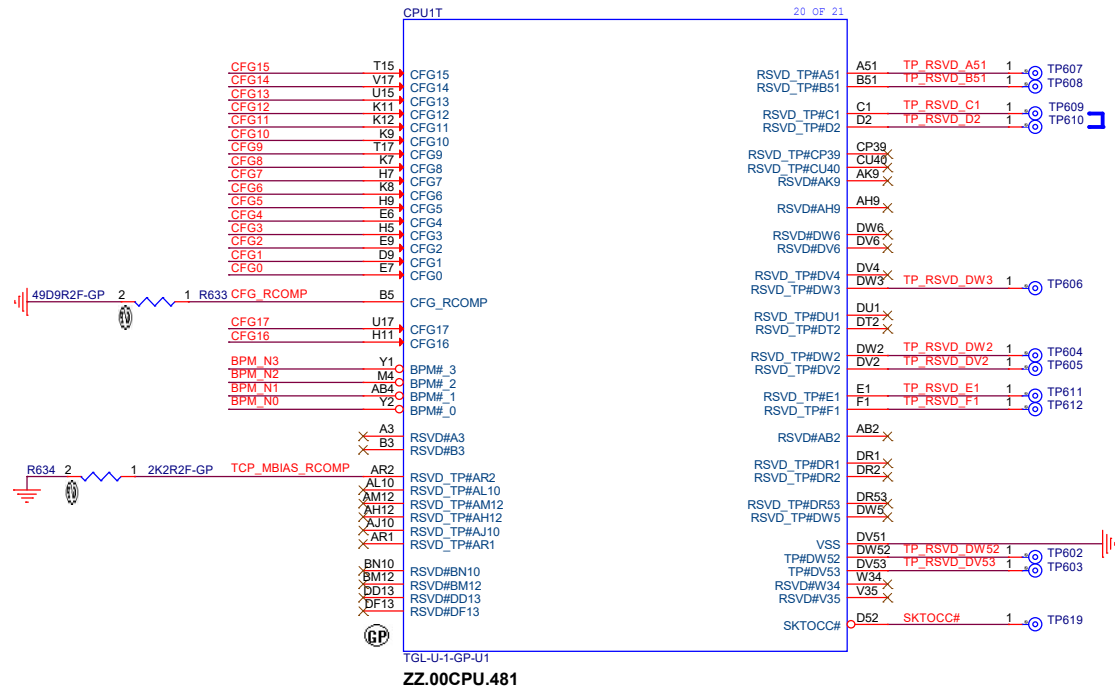
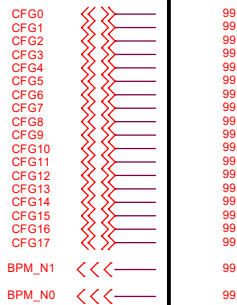
TC_RCOMP_P AN2
TC_RCOMP_N AN1
DSI_DE_TE_2 M8
DDI_RCOMP AB1
DISP_UTILS/DSI_DE_TE_1 CE4

Multi

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title CPU (DDI/EDP)			
Size A3	Document Number SouthPeak15 TGL	Rev SB	
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Main Func = CPU



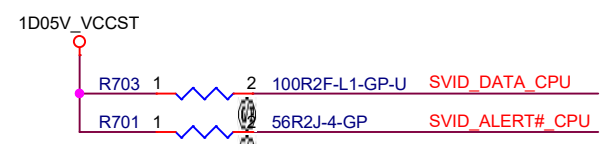
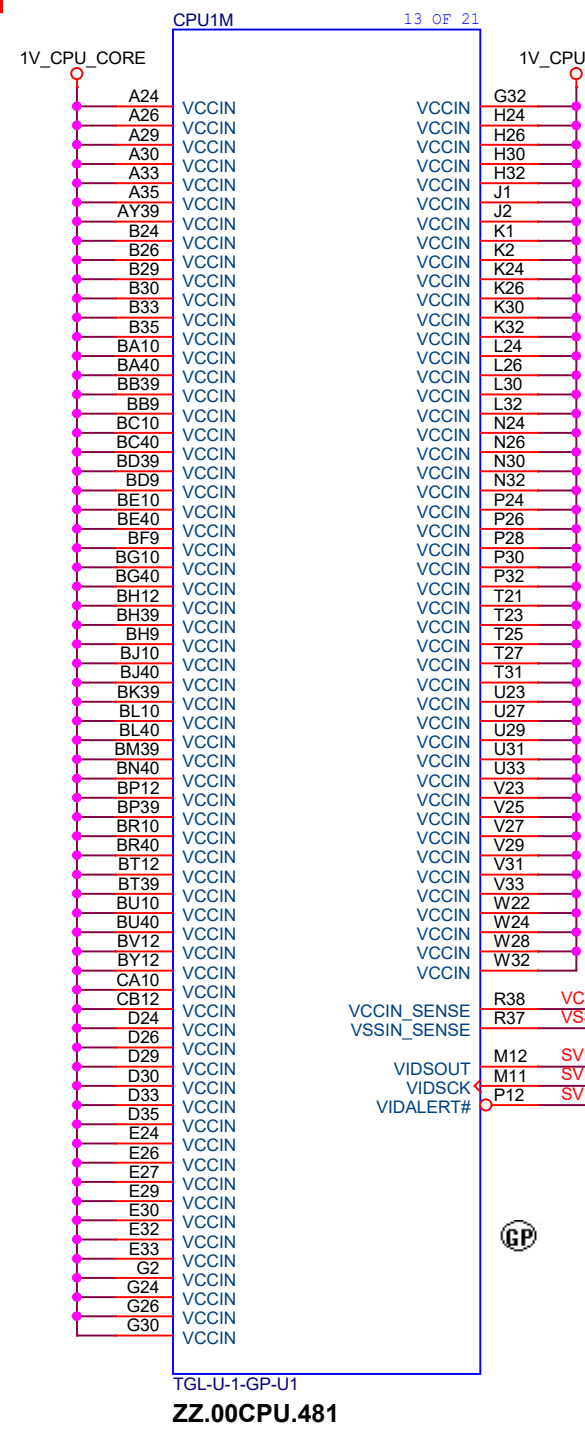
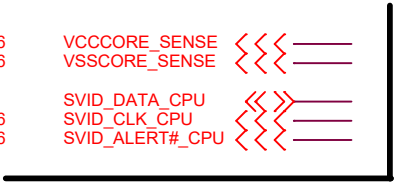
CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

Multi



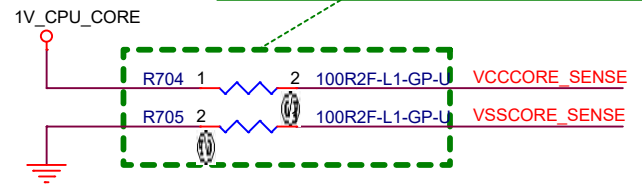
Title			CPU (CFG/IST)		
Size	Document Number	SouthPeak15 TGL			Rev
A3					SB
Date:	Friday, April 24, 2020	Sheet	6	of	106

Main Func = CPU




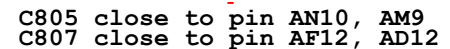
Layout note:
Length matchin 25mil, and close SOC in 2inch "


Layout Note:
1. Place close to CPU within 2"
2. VCC_SENSE/ VSS SENSE impedance=50 ohm
3. Length match<25mil



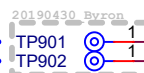
Multi

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Title CPU (VCORE/VID)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
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Title CPU (VCCGT/VCCIO/VDDQ/VCCSA)			
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PCH_IST_TP1
PCH_IST_TP0

DF53
DF52
DT52
DU53
DF50
DF49
CY30
CY15
D4
A6
A4

CPU1S
RSVD#DF53
RSVD#DF52
PCH_IST_TP1
PCH_IST_TP0
RSVD#DF50
RSVD#DF49
RSVD_TP#CY30
RSVD_TP#CY15
RSVD_TP#D4
IST_TP1
IST_TP0

RSVD#C53
RSVD#T35
RSVD#E53
RSVD#CF39
RSVD#U35
RSVD#F53
RSVD#B53
RSVD#AP9
RSVD#A52
RSVD_TP#BF12
RSVD_TP#V21
RSVD_TP#W20
RSVD_TP#U37
RSVD_TP#CD39
RSVD_TP#U21
RSVD#CB39
RSVD_TP#BB12
RSVD_TP#W37
RSVD_TP#AY12
RSVD_TP#W38
RSVD_TP#U38
RSVD_TP#CY28

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IST_TP1
IST_TP0



TGL-U-1-GP-U1
ZZ.00CPU.481

CPU1D 4 OF 21

DV24
DW47
DW49
A48
RSVD#DV24
RSVD#DW47
RSVD#DW49
RSVD#A48



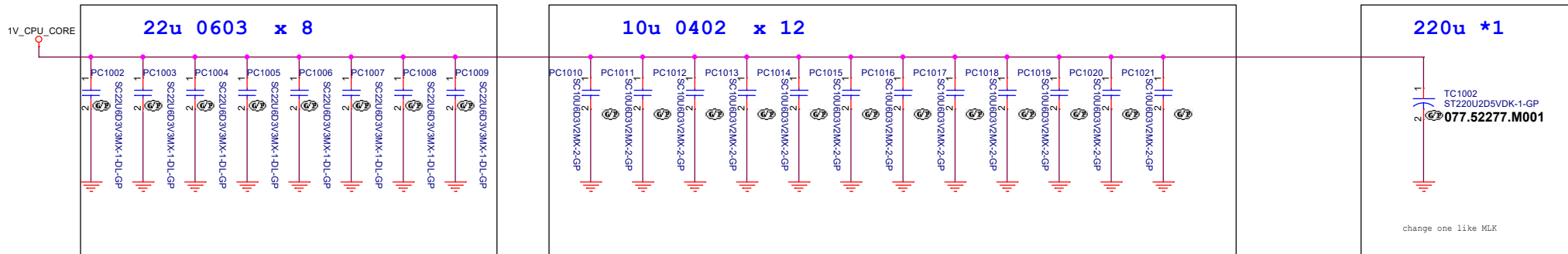
TGL-U-1-GP-U1
ZZ.00CPU.481

Multi

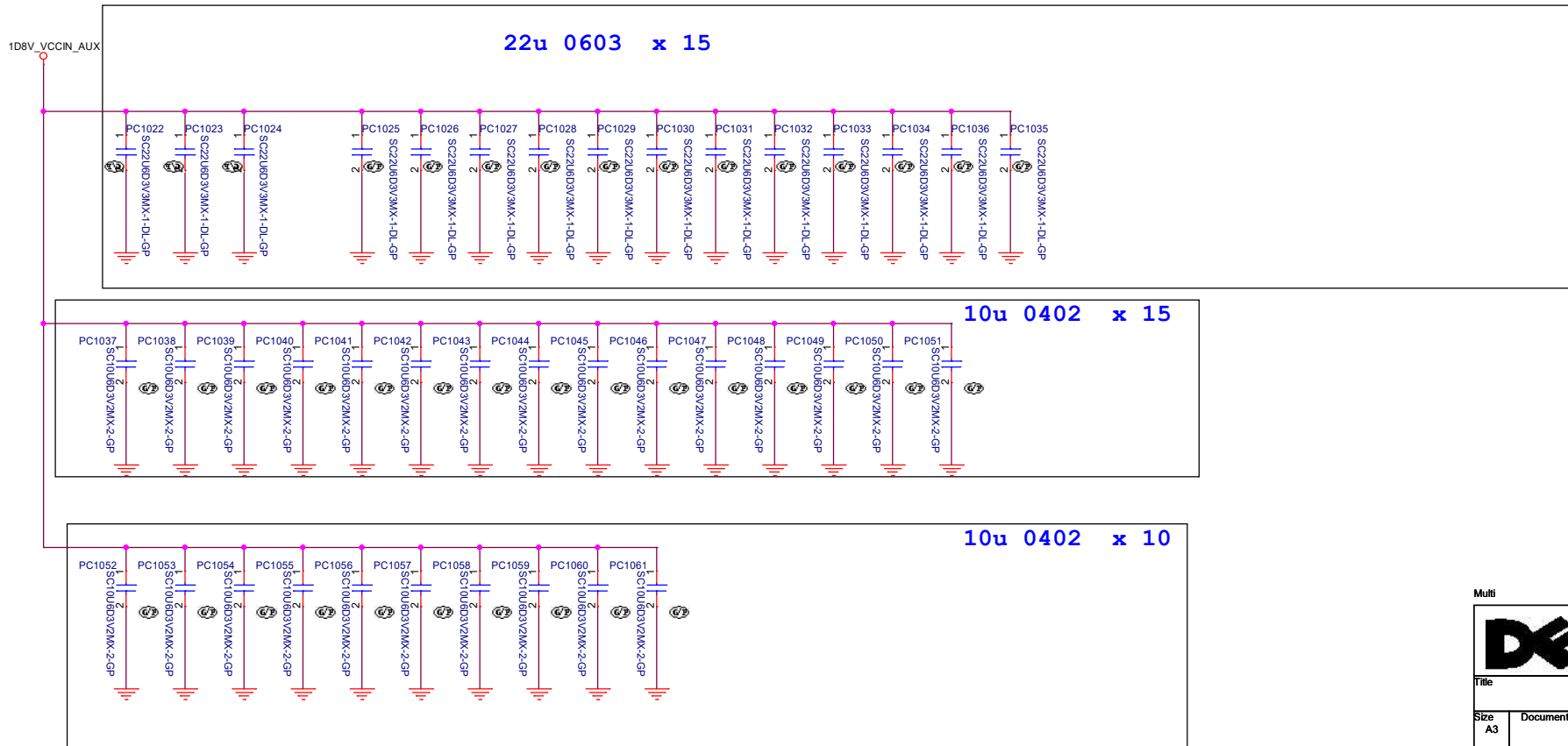
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Title CPU (RSVD)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
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Main Func = CPU

1V_CPU_CORE (VCCIN)



VCCIN_AUX



Multi



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (CORE Power Cap1)

Size
A3

Document Number

SouthPeak15 TGL

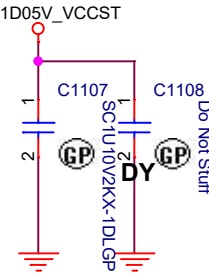
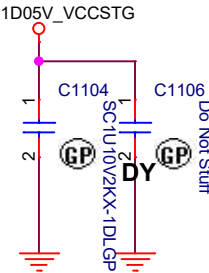
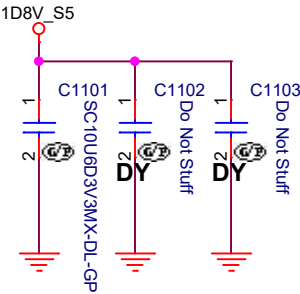
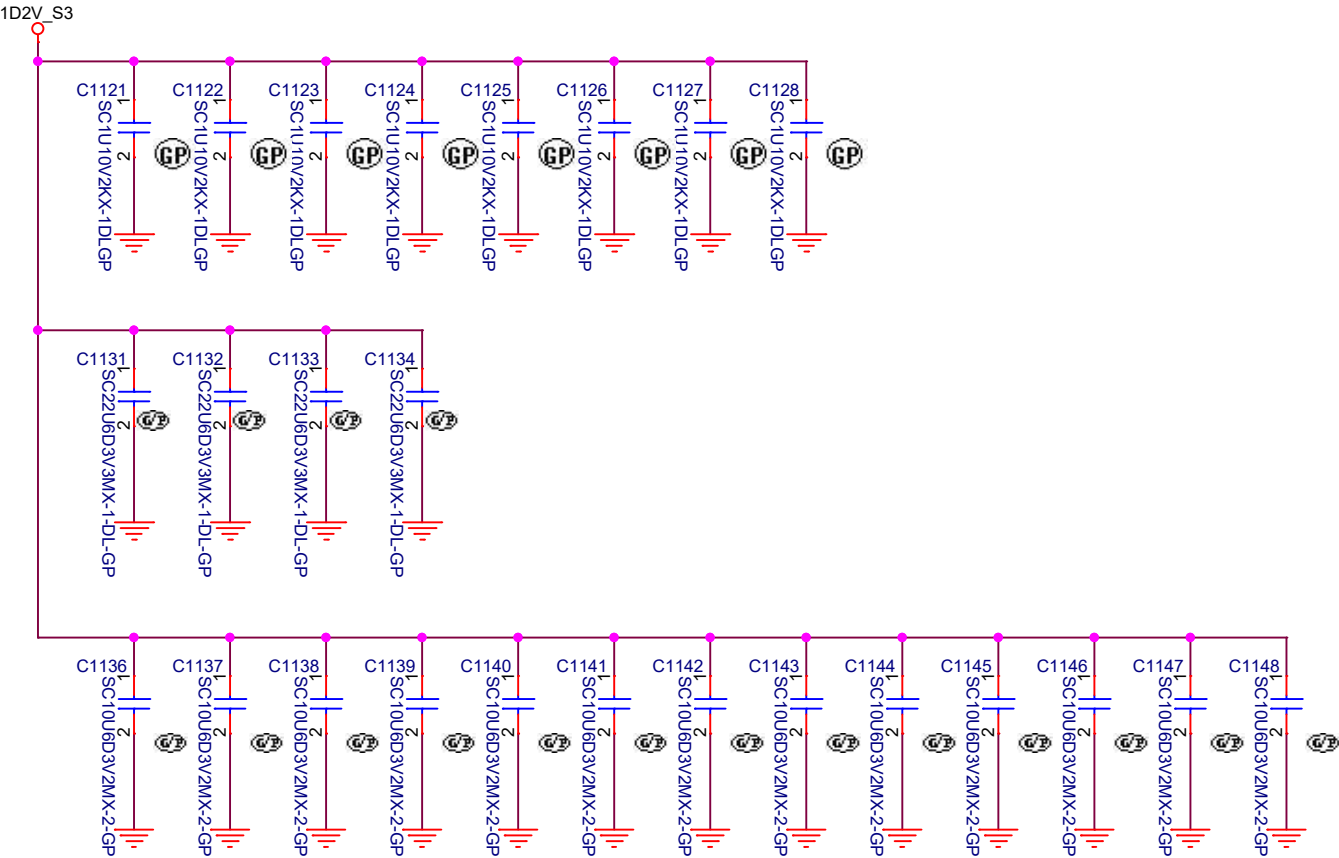
Rev
SB

Date: Friday, April 24, 2020


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Main Func = CPU

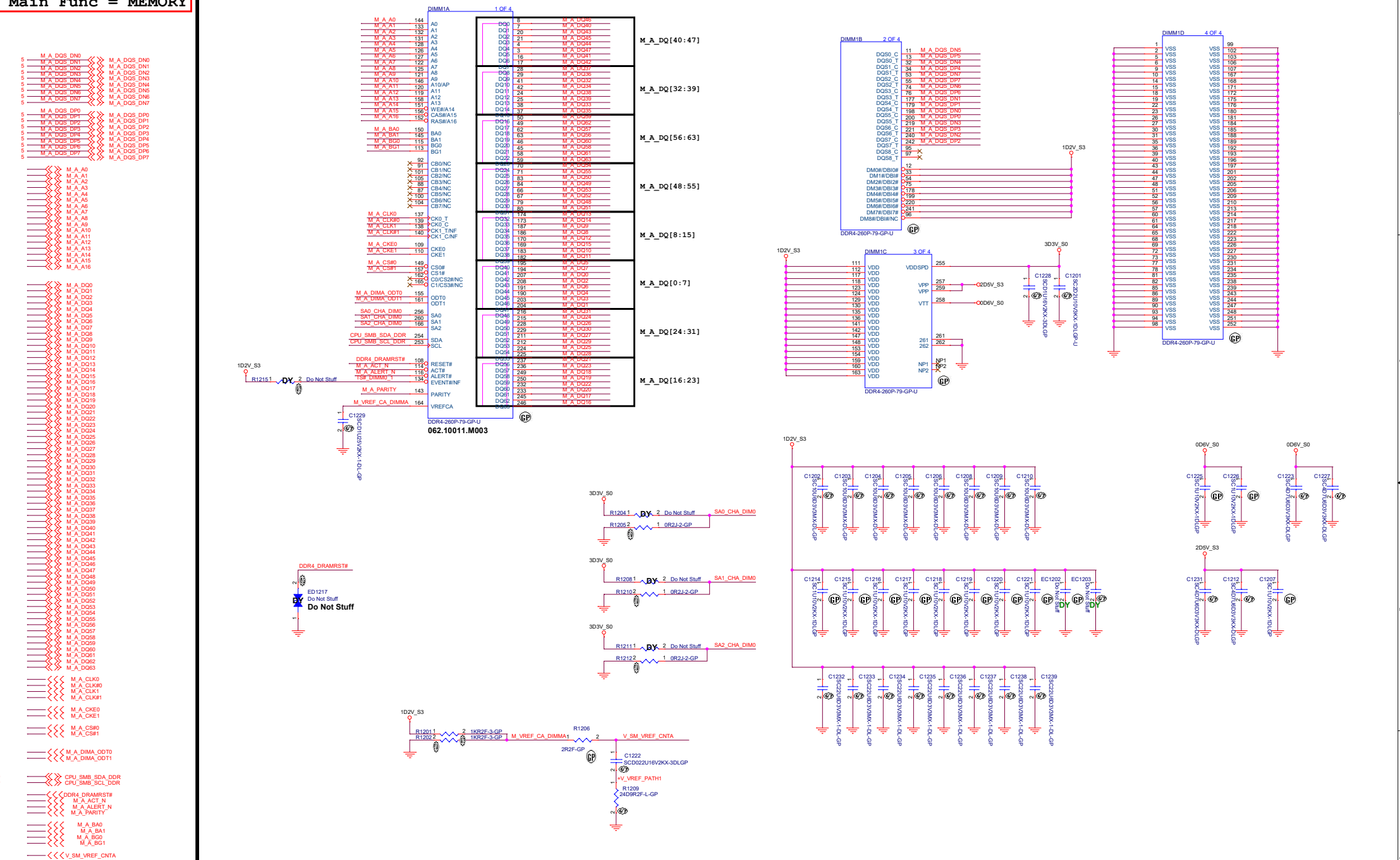
VDDQ



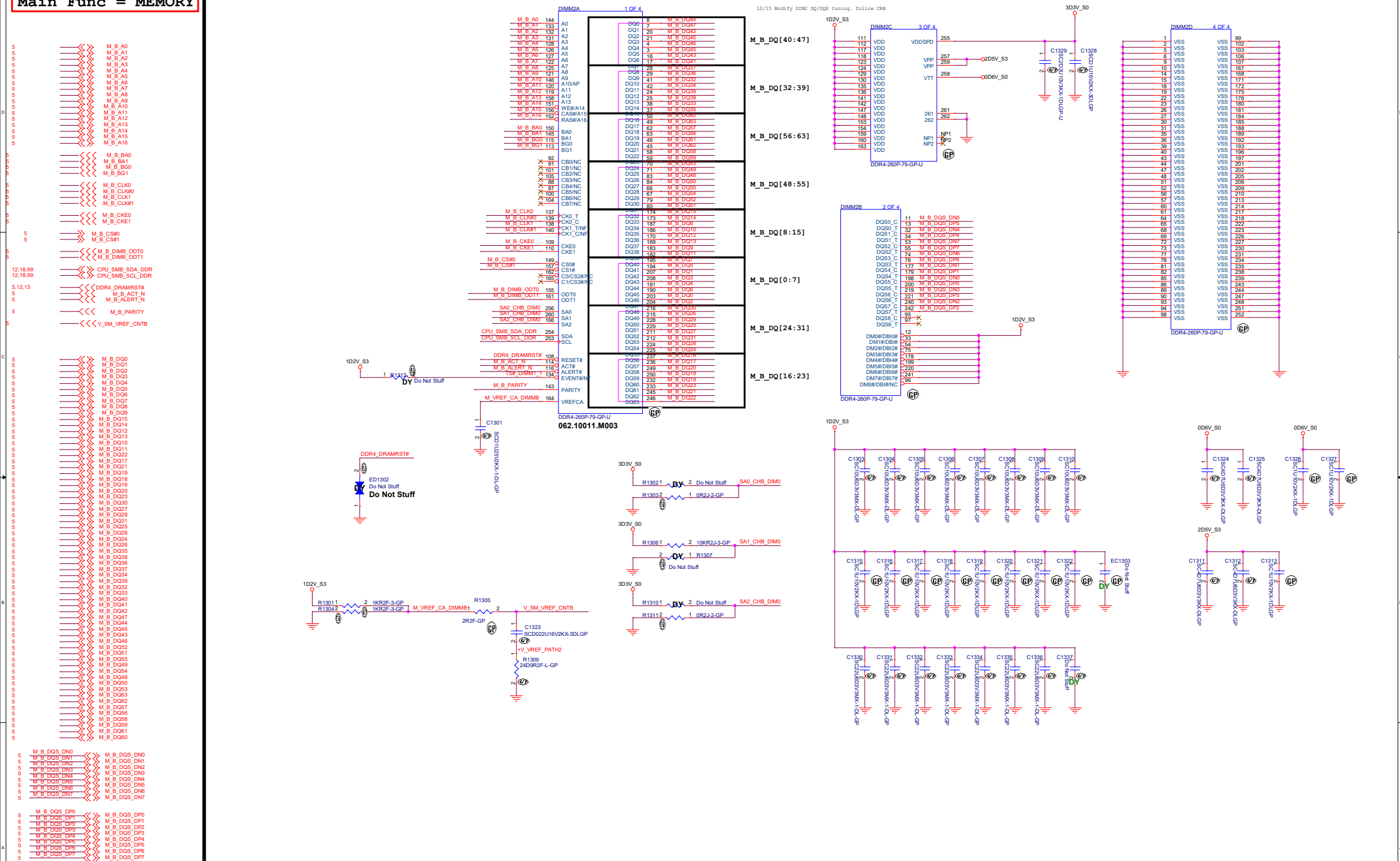
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CPU (Power Cap2)			
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Main Func = MEMORY




Main Func = MEMORY



(Blanking)

Multi

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Title					
DDR (RSVD) (DDR4-CHA1)					
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18.6899 SPI_SI_CPU <<<—
18.6899 WP_CPU <<<—
18.6899 HOLD_CPU <<<—

CNV_RGL_DT >>>—
GPP_C5 <<<—
GPP_E6 <<<—
HDA_SDO <<<—
TBT_LSX0_RXD >>>—

3.99 DBG_PMODE <<<—
4.71 TBT2_LSX0_RXD <<<—
18 GPP_E10 <<<—

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)		
21.61									
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE		
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE		
GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10	GPP_E11	
Schematic									
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)			
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED			

Original Ref.

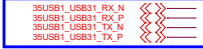
GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EO LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PU 20K	BOOT HALT HIGH - DISABLED LOW: ENABLED NO INTERNAL PUPD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PUPD	CPU/SSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PU 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PUPD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PU 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PUPD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD
TBT LSX #1	TBT LSX #2	TBT LSX #3	A0	GPP_E10	GPP_E11		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PUPD				

Main Func = PCH

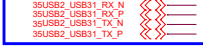
#543016:
220 nF nominal capacitors are recommended for Gen 3
100 nF nominal capacitors are recommended for Gen 2

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

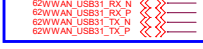
USB3.1 PORT1



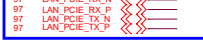
USB3.1 PORT2



WWAN



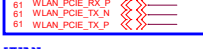
LAN



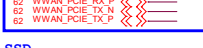
CARD



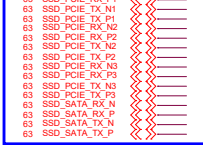
WLAN



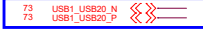
WWAN



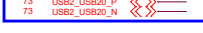
SSD



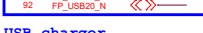
Type C USB 1



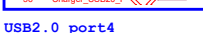
Type C USB 2



FP



USB charger



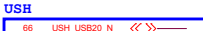
USB2.0 port4



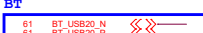
CAMERA



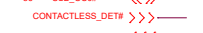
WWAN



USH



BT



CONTACTLESS_DET#



GPU_G06_FB_EN



m2280_PCIE_SATA#



M2280_DEVSUP



SSD

LAN

CARDREADER

WLAN

WINDOS WWAN

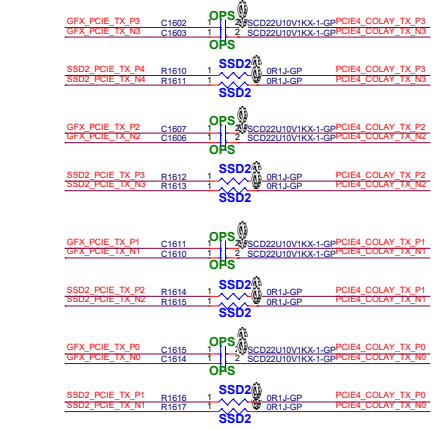
UBUNTU WWAN

USB4 Type A port2

USB3 Type A port1



TGL-U1-GRU1
ZZ.00CPU.481



SSD2



SSD2



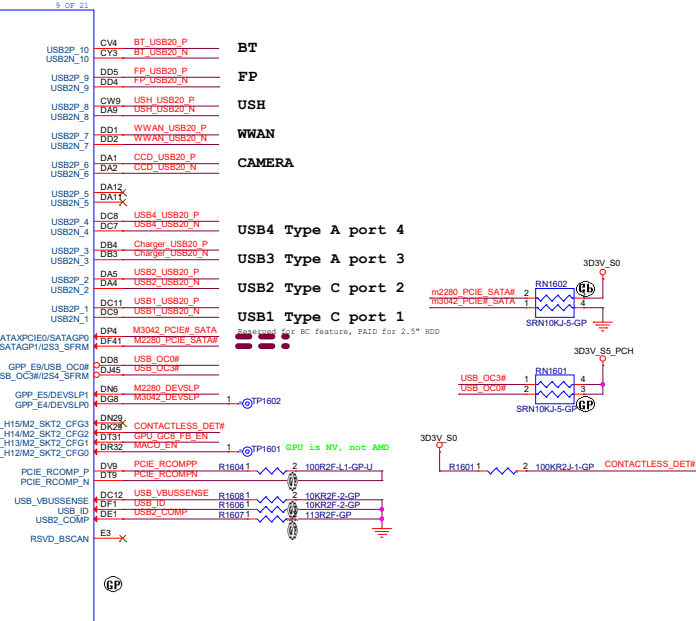
SSD2



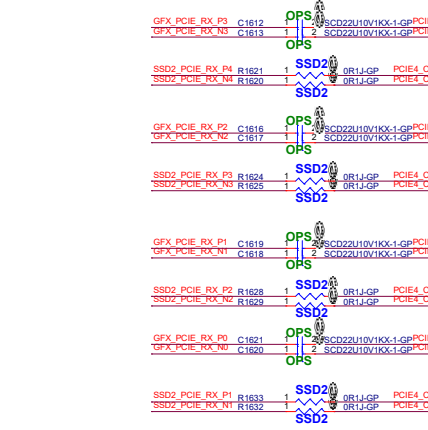
SSD2



SSD2



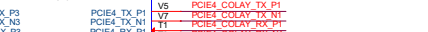
TGL-U1-GRU1
ZZ.00CPU.481



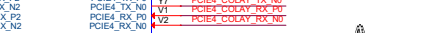
SSD2



SSD2



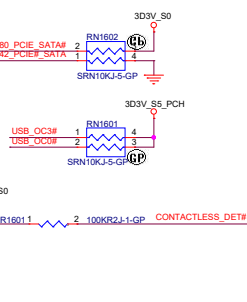
SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



SSD2



Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

```

24.58 SIO_SLP_SUS# <<<
28 SIO_SLP_SUS# <<<
51.08 SIO_SLP_SUS# <<<
24.40.68 SIO_SLP_S3# <<<
68 SIO_SLP_S4# <<<
68 SIO_SLP_S5# <<<
68 SIO_SLP_S0# <<<

40 SIO_SLP_WLAN# <<<
40 SIO_SLP_LAN# <<<

68.99 SYS_RESET# <<<

PCH_DPWR0K >>>
PCH_DPWR0K >>>
SYS_PWROK_R >>>

RTC_INTRUDET# >>>

SIO_PWRBST# >>>

24 AC_PRESENT >>>

97 LAN_WAKE# <<<

24.62 PCH_PCIE_WAKE# <<<

97 PM_LANPHY_ENABLED <<<

TRCSTRT_ON >>>

RSMRST#_KBC >>>

ALL_SYS_PWRGD >>>

33.61.68M_PLCRST#_RIGHT <<<
63.71.68M_PLCRST#_LEFT <<<

40.91 CPU_C10_GATE# <<<

20.27 SPKR <<<

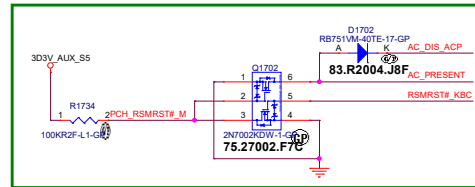
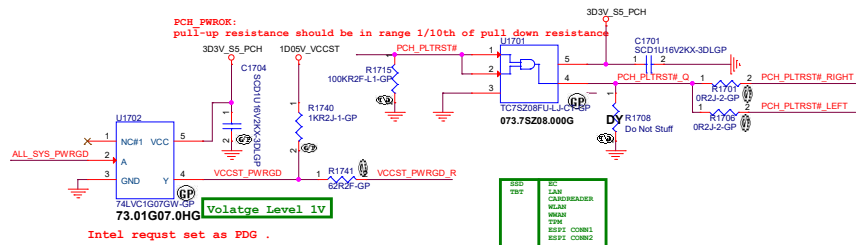
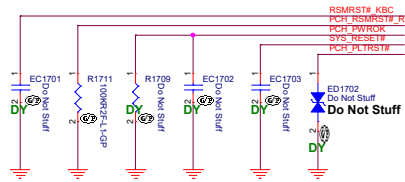
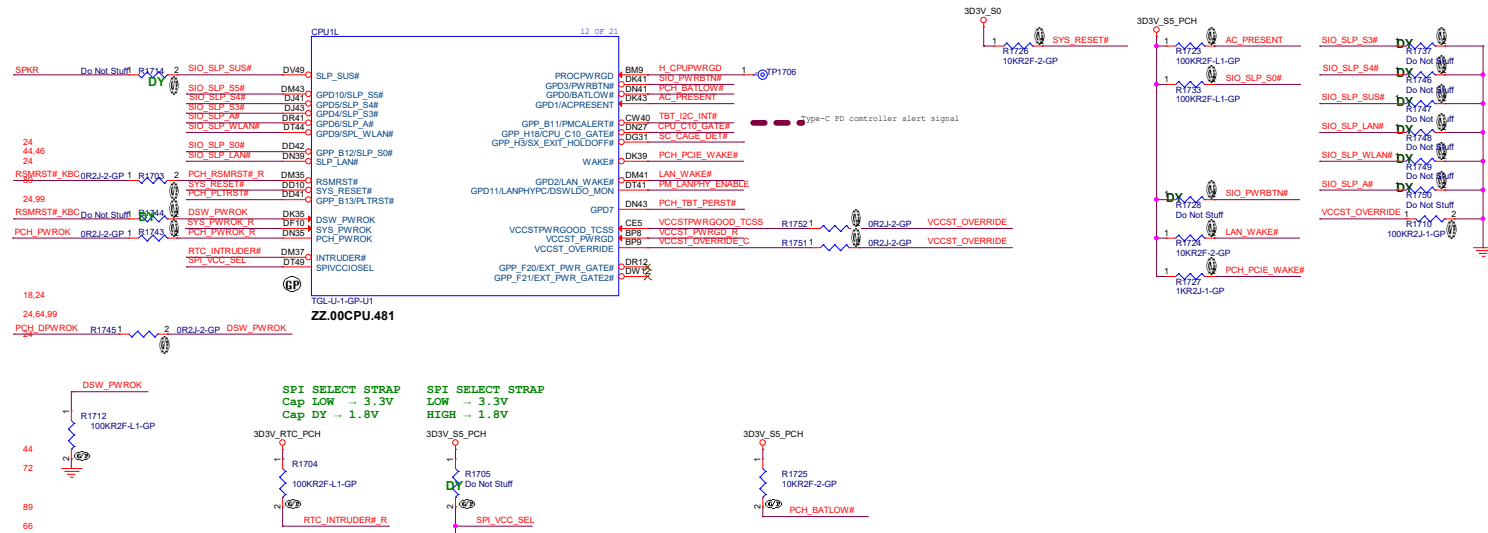
40 VCCST_OVERRIDE <<<
AC_DIS_ACP >>>

TBT_LCN_INT# >>>

71 PCH_TBT_FERST# <<<
RTC_INTRUDET# >>>

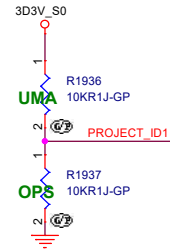
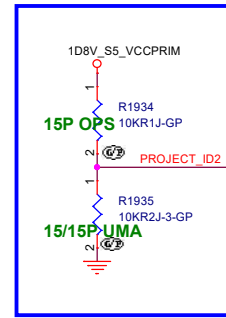
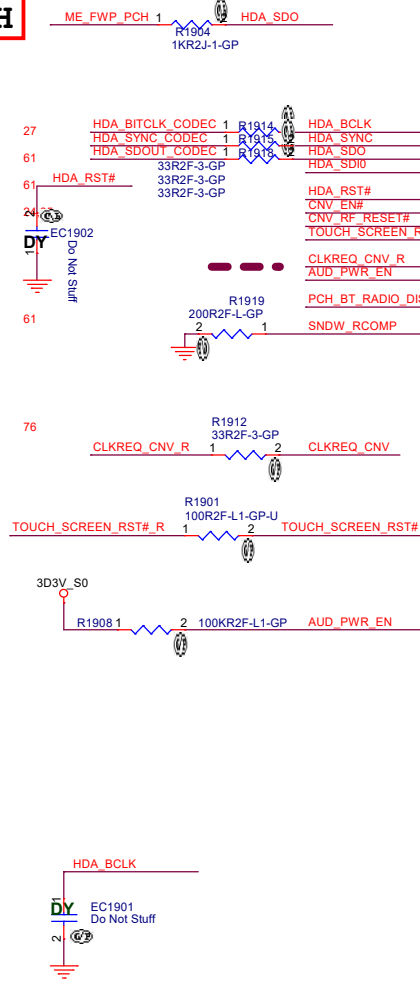
SC_CAGE_DET# >>>

```



Main Func = PCH

27,9HDA_SDI0 <<<<
 27 HDA_SDOOUT_CODECC <<<<
 27 HDA_SYNC_CODECC <<<<
 27 HDA_BITCLK_CODECC <<<<
 15 HDA_SDO <<<<
 HDA_RST# <<<<
 PCH_BT_RADIO_DIS# <<<<
 CLKREQ_CNV >>>>
 DGPU_PWROK <<<<
 55TOUCH_SCREEN_RST#_R <<<<
 61 CNV_EN# <<<<
 68 ME_FWP_PCH <<<<
 CNV_RF_RESET# <<<<
 55 BLON_OUT_R <<<<
 96 HDA_BCLK <<<<
 DGPU_HOLD_RST# >>>>



	15 (i3, i5, i7)		15P (i5, i7)	
	UMA	DSC (N155-G5)	UMA	DSC (QN20-M1)
Accelerometer sensor on MB	LNG2DMTR (8-bit)	LNG2DMTR	LNG2DMTR	LIS2DW12TR (16-bit)
GPP_R5 (PROJECT_ID1)	1	0	1	0
GPP_S4 (PROJECT_ID2)	0	0	0	1

Multi



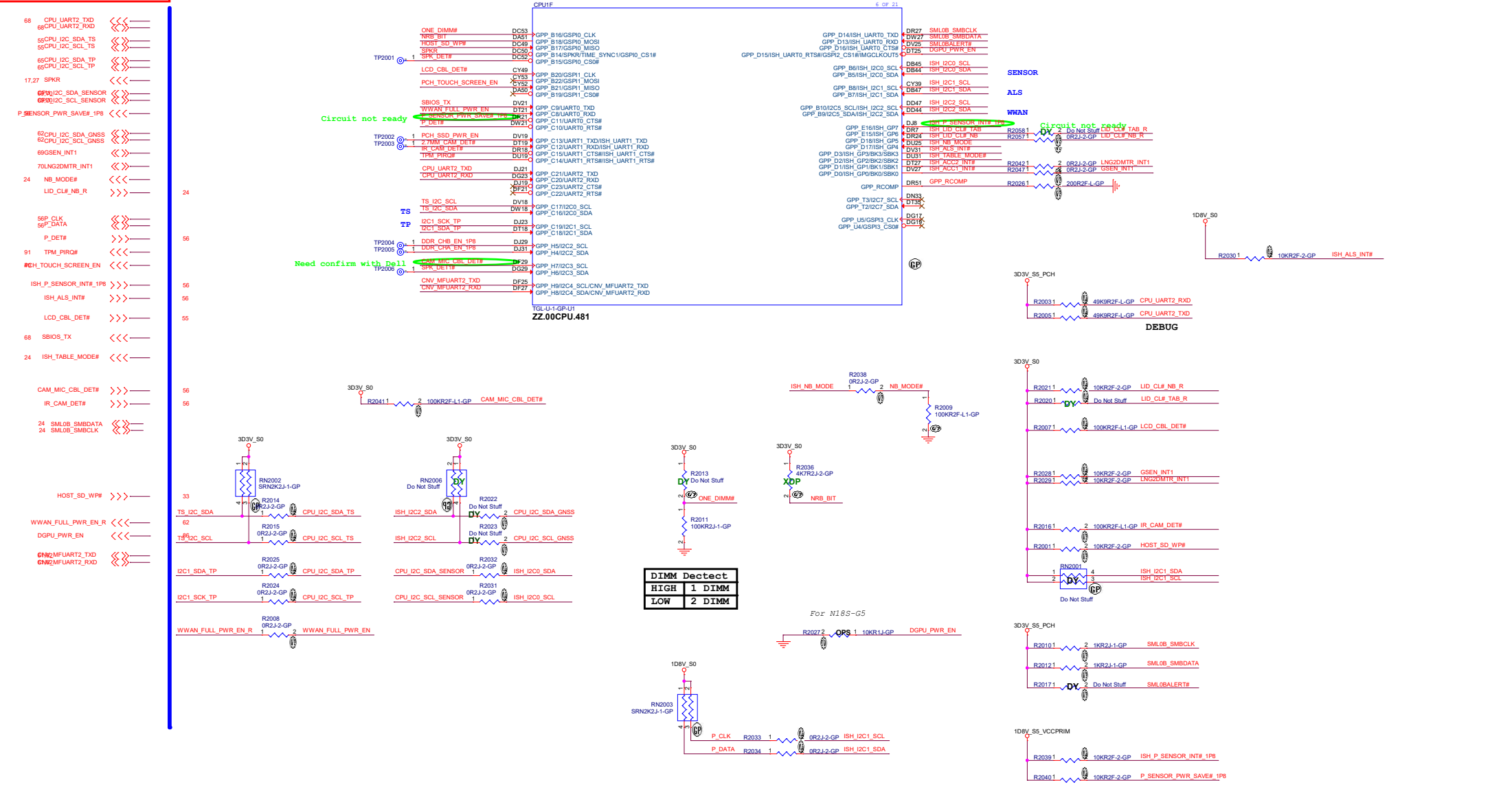
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsin 221, Taiwan, R.O.C.

Title **CPU (HDA/I2S/SD/DMIC)**


Size A3 Document Number **SouthPeak15 TGL** Rev **SB**

Date: Friday, April 24, 2020 Sheet 19 of 106

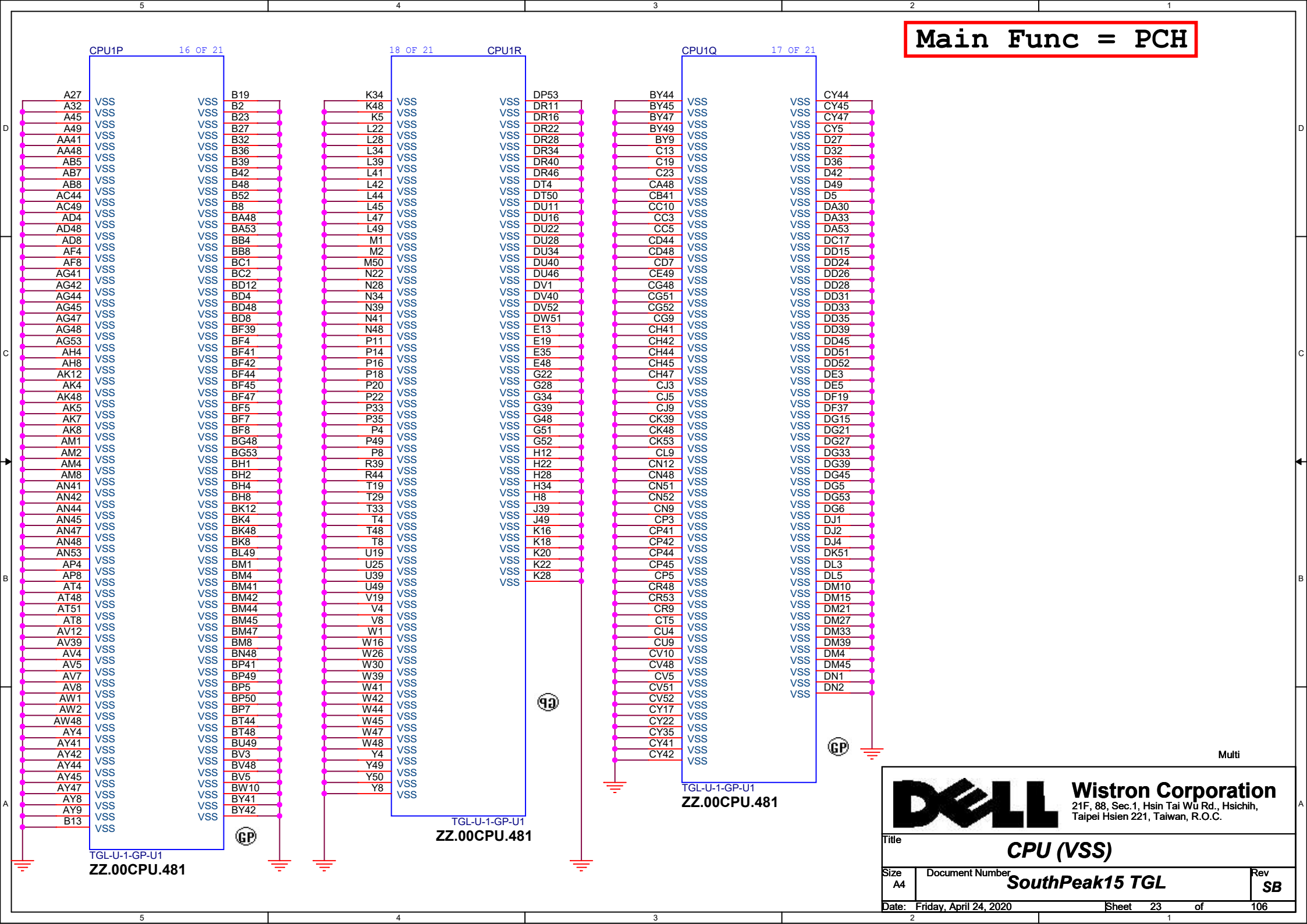
Main Func = PCH




[illegible]

	<p style="margin: 0;">Wistron Corporation</p> <p style="margin: 0;">21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title</p> <p style="text-align: center; font-size: 1.2em;"><i>CPU (EMMC/CNVi)</i></p>		
<p>Size</p> <p style="text-align: center;">A4</p>	<p>Document Number</p> <p style="text-align: center; font-size: 1.2em;"><i>SouthPeak15 TGL</i></p>	<p>Rev</p> <p style="text-align: center;">SB</p>
<p>Date: Friday, April 26, 2020</p>		<p>Sheet 21 of 106</p>

Main Func = PCH





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Title

CPU (VSS)

Size
A4

Document Number
SouthPeak15 TGL

Rev
SB

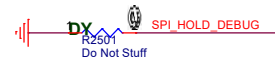
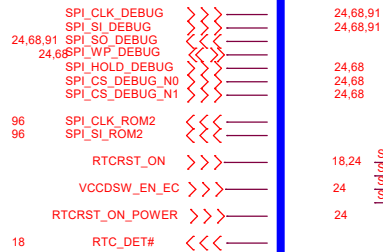
Date: Friday, April 24, 2020

Sheet 23 of 106

Main Func = EC



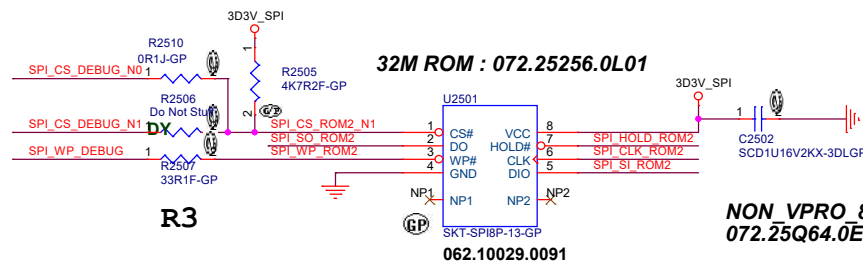
SYSTEM SPI ROM



Non-vPRO configs - 16MB (UI)
Winbond W25Q128JVS1Q; MXIC: MX25L12873FM; GigaDevice:
GD25B127D

UD128-128L
If more than 3 sources are required then these parts can be considered:
Spanion: S25FL128L; Micron: MT25QL128ABA1ESE-0SIT

vPRO Configs: 32MB
Winbond W25Q256JV, Gigadevice GD25Q256C, Cypress S25FL256L



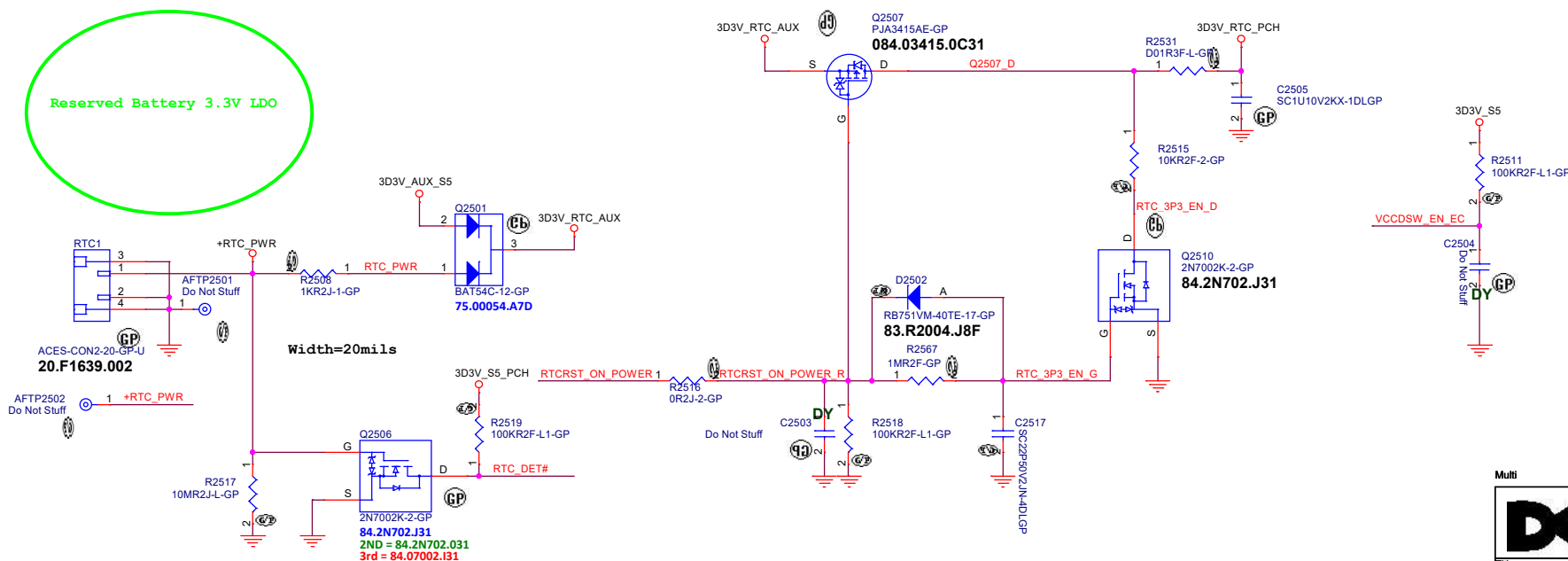
NON_VPRO_8MB 手動換料
072.25Q64.0E03

WinBond		W50N (8x6)		8-Pin SOIC 208-mil	
ROM size		Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
8M Byte	64M bit	072.25Q64.D003	W25Q64V2EIQ	072.25Q64.D010	W25Q64V5SIQ
16 M Byte	128 M bit	072.25128.0A11	W25Q128V1EIQ	072.25128.0B51	W25Q128V5SIQ
32 M Byte	256 M bit	072.25256.D001	W25Q256V1EIQ		N/A

MXIC		W5CON (8x6)		8-pin SOP (200mil)	
ROM size		Wistron Part No.	Vender Part No.	Wistron Part No.	Vender Part No.
8M Byte	64M bit	072.25643.0B01	MX2561633F2J1	072.25647.000D	MX2561673FM21-08G
16 M Byte	128 M bit	XX	XX	072.12873.0001	MX25612873FM21-08G
32 M Byte	256 M bit	072.25673.0003	MX25125673G241-08G	072.25673.0001	MX25125673GM21-08G

GRIAGEVICE		WSOIN (8x6)		SOP8 208MIL	
ROM size		Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
8M Byte	64M bit	072.02564.0P01	GD25B64C1GR	072.25B64.0C01	GD25B64C1GR
16 M Byte	128 M bit			072.25127.0001	GD25B127DSGR
32 M Byte	256 M bit	072.25656.0B03	GD25B256DYGR		

X09 design DS3_Non-DS3 with RTC power gating



Multi



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Title	Flash/RTC
-------	------------------

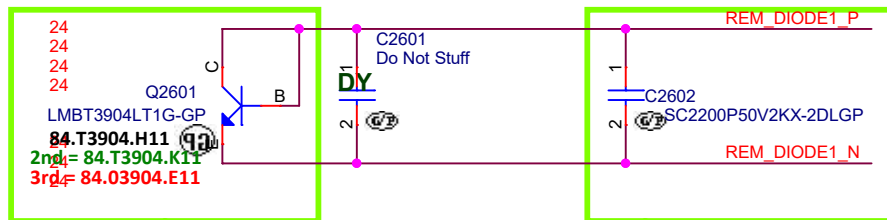
Size A3	Document Number SouthPeak15 TGL	Rev SB
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Main Func = Thermal / FAN

REM_DIODE1_P
REM_DIODE1_N
REM_DIODE2_P
REM_DIODE2_N

REM_DIODE4_P
REM_DIODE4_N
PWM_FAN1
TACH_FAN1

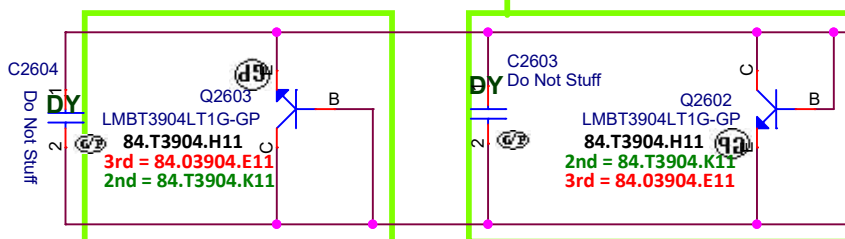


Layout Note: Place to CPU

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

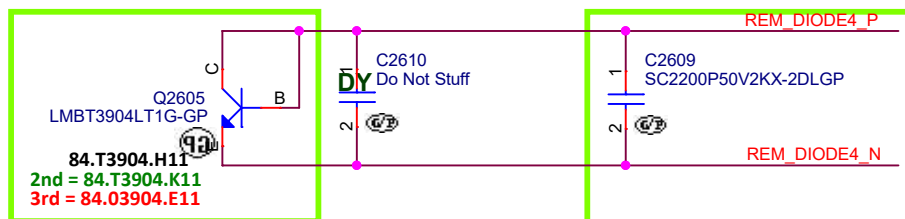
Layout Note: Close to WWAN/2nd SSD



Layout Note: Place to DIMM

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

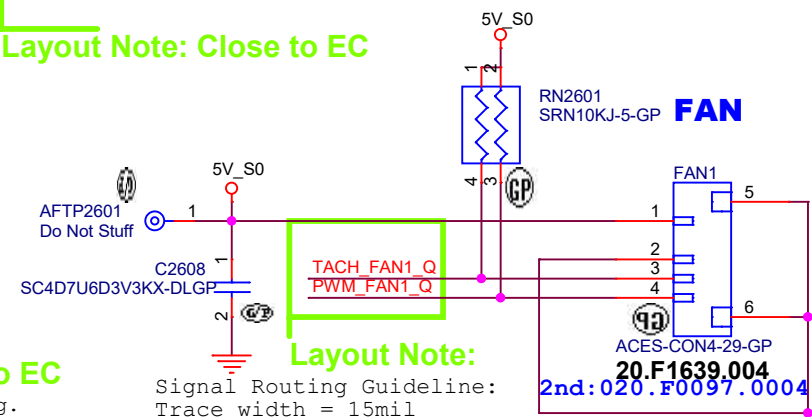
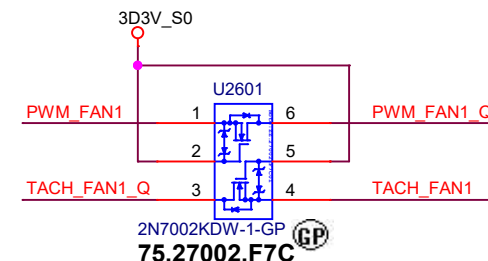


Layout Note: Place to V.R

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

5105 Channel	Location
DP1/DN1	CPU (Q2601)
DP2/DN2	WWAN (Q2602)
DN2a/DP2a	DDR (Q2603)
DP4/DN4	V.R (Q2605)



Layout Note:

Signal Routing Guideline:
Trace width = 15mil

TACH_FAN1_Q 1
PWM_FAN1_Q 1

AFTP2602 Do Not Stuff
AFTP2603 Do Not Stuff

Multi



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Taipei Hsien 221, Taiwan, R.O.C.

Title **INT IO (Thermal/Fan)**

Size A4 Document Number **SouthPeak15 TGL**


Rev **SB**

Date: Friday, April 24, 2020

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5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

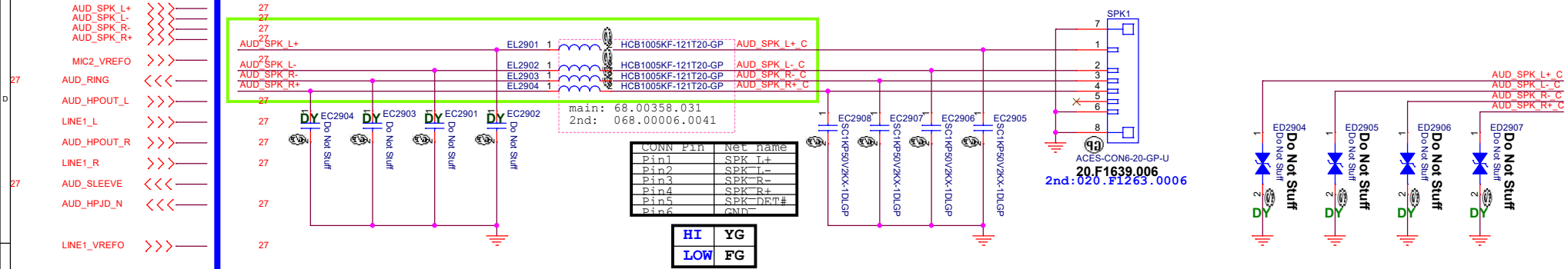
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (RSVD) (Audio AMP)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 28	of 106

Main Func = Audio

Layout Note:

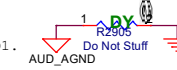
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

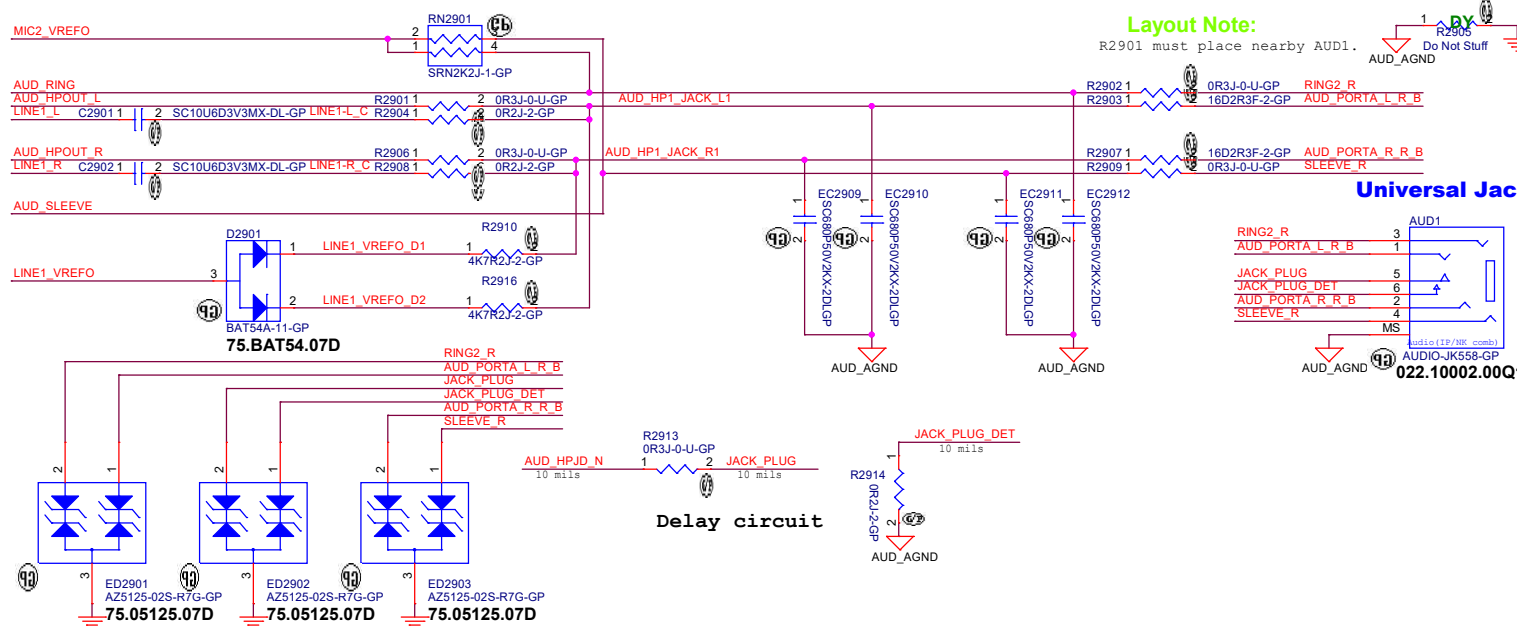
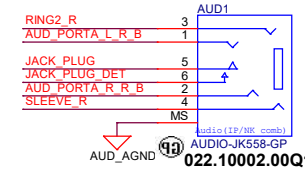


Layout Note:

R2901 must place nearby AUD1.




Universal Jack



Multi


5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

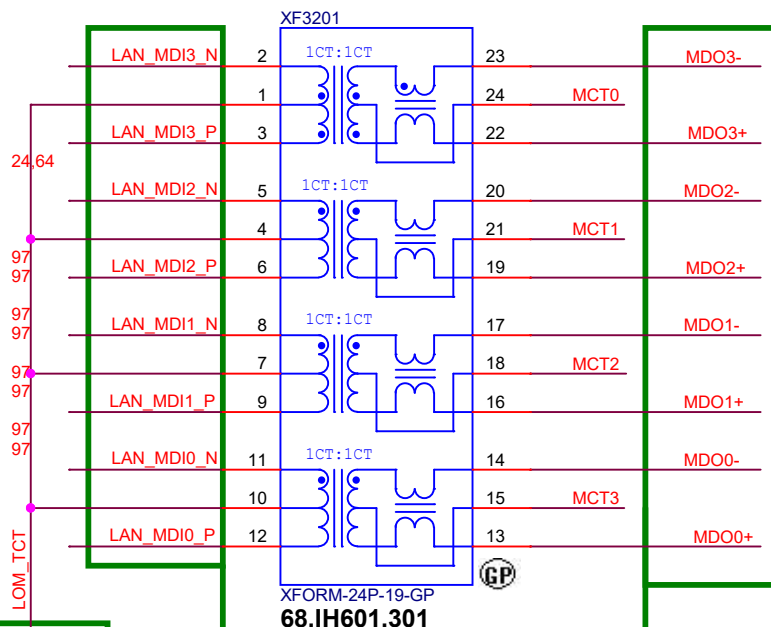
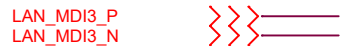
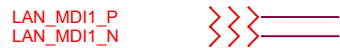
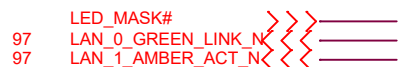
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (HP/SPK/MIC Jack)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 30 of	106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

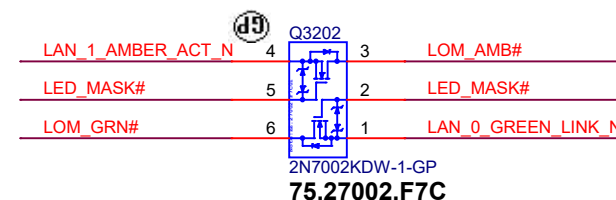
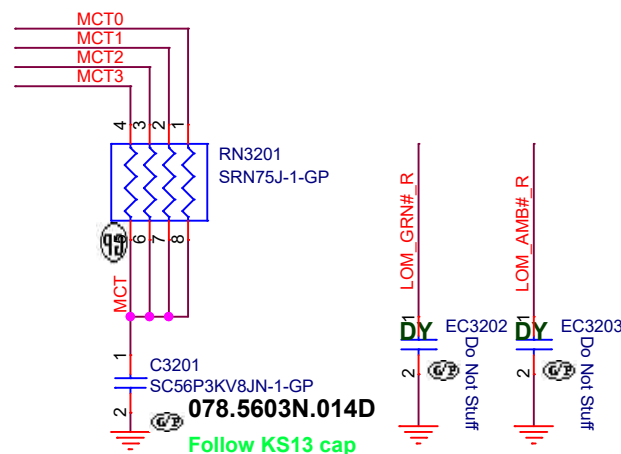
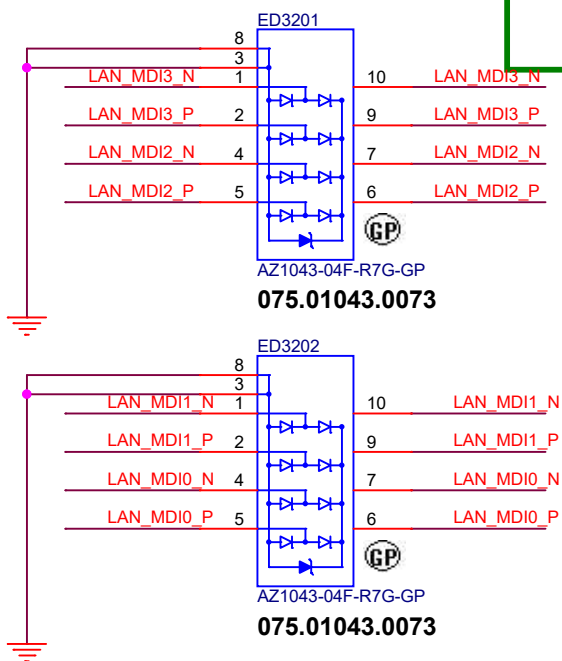
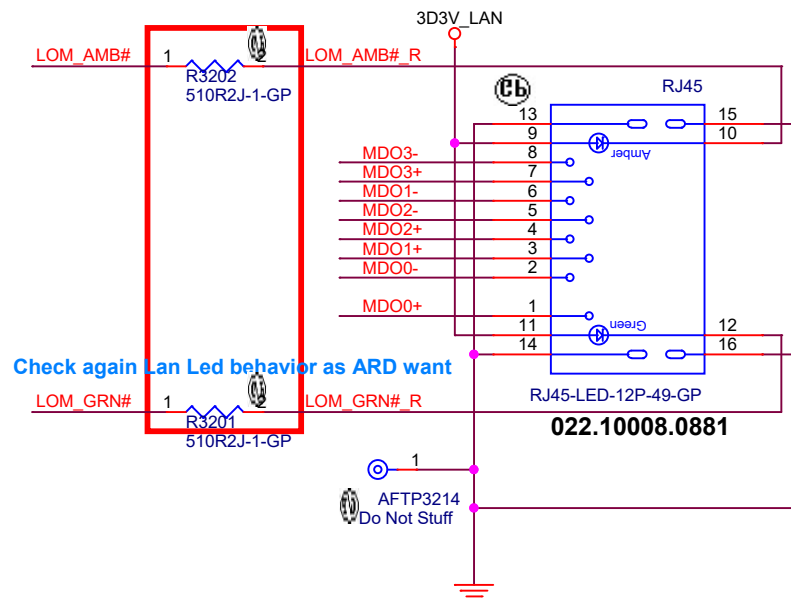
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LAN (RSVD)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 31 of	106

Main Func = LAN



Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF



- **LED0 (010):** Green = Indicates Link connection established (located on left-hand side of connector)
- **LED1 (011):** Amber = Blinking when network activity (located on right-hand side of connector)



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Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN (RSVD) (RJ45+Transformer)
-------	--------------------------------------

Size
A4

Document Number:

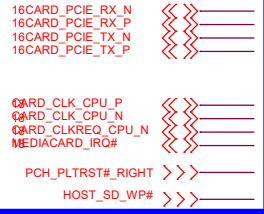
SouthPeak15 TGL

Rev
SF

Main Func = Card Reader

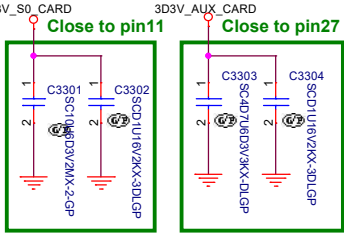
3D3V_S0_CARD

850mA

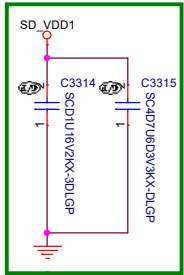
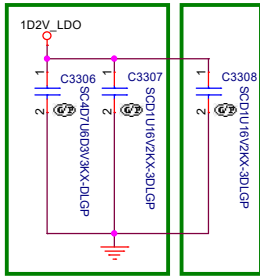


Layout Note:

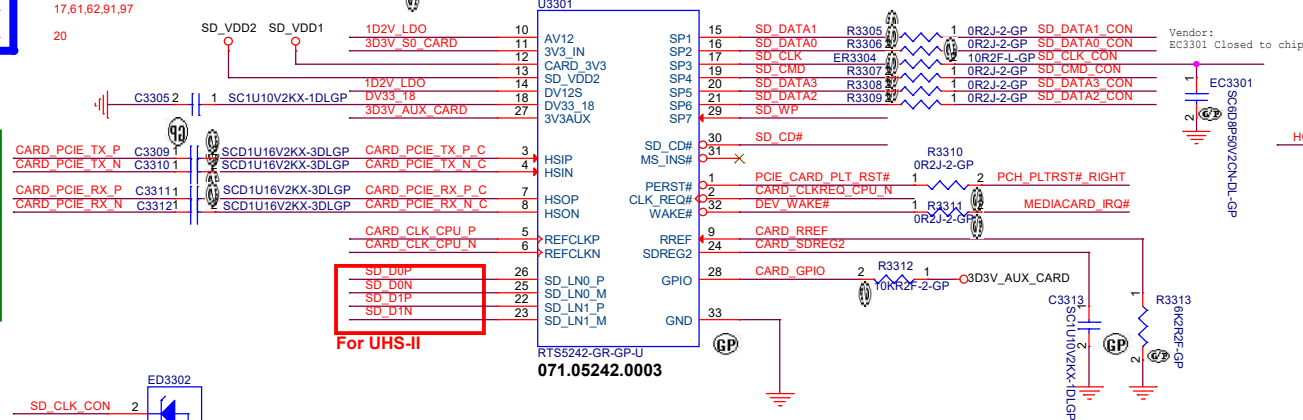
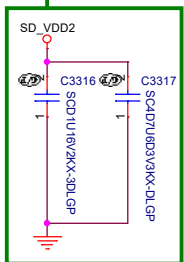
17,61,62,91,97
20



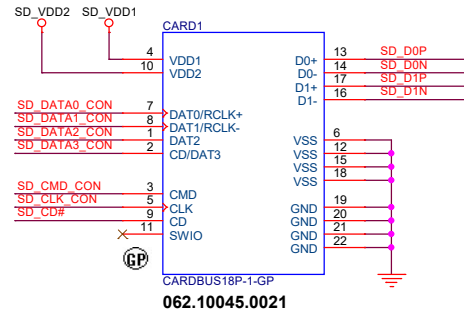
Close to pin14 Close to pin10



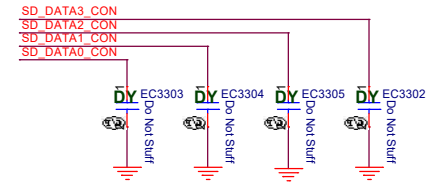
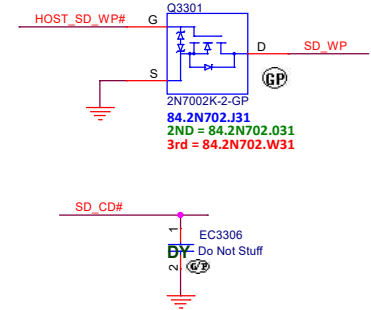
Layout Note:Close to Card Reader CONN



For UHS-II



SD_CLK_CON 96
SD_DATA0_CON 96
SD_DATA1_CON 96
SD_DATA2_CON 96
SD_DATA3_CON 96
SD_CMD_CON 96



Multi



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CARDREADER (SDIO/SD Conn)


SouthPeak15 TGL

SB

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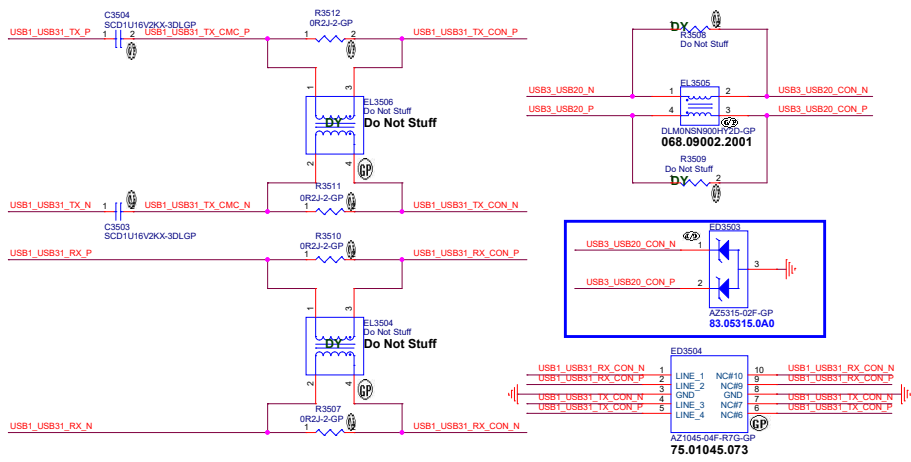
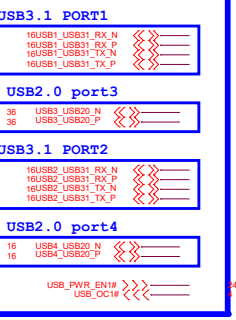
5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

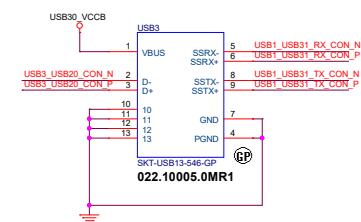
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB (RSVD) (USB2.0 CONN)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 34	of 106

Main Func = USB 3.0

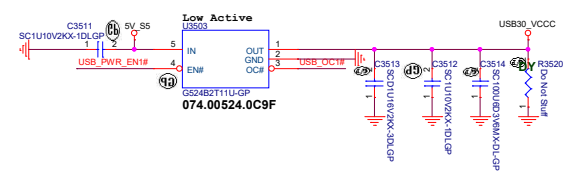
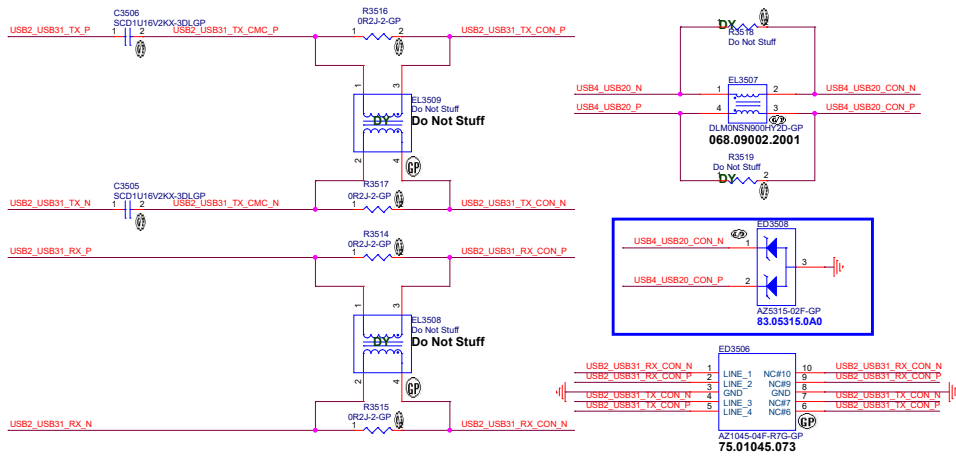
USB3/USB31-1/USB20-3/PowerShare



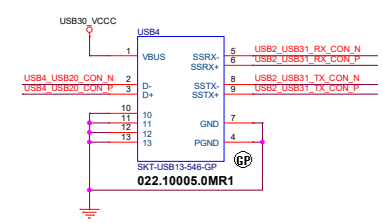
EXT Port1 Right Side, Support Power Share



USB4/USB31-2/USB20-4



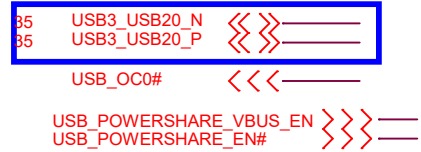
EXT Port1 Right Side, Support Power Share



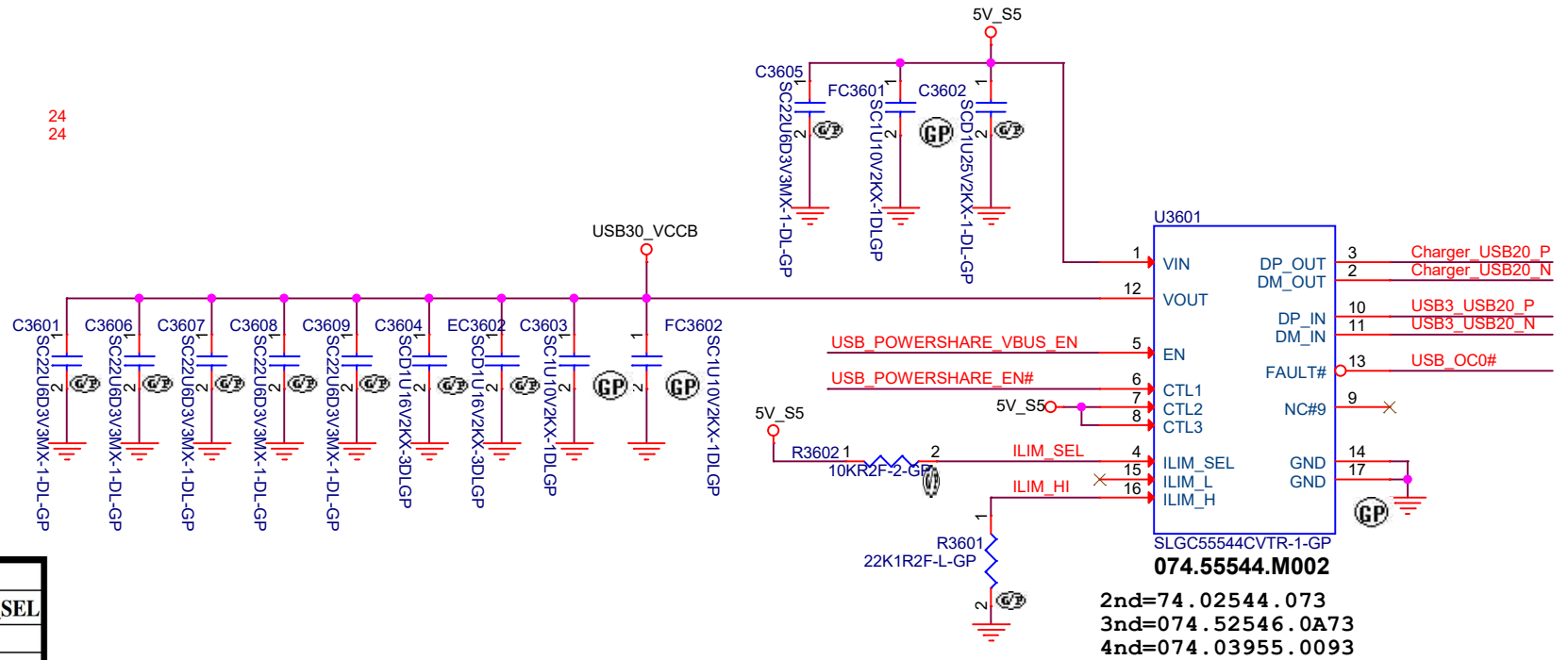
Main Func = USB Charger

support power share on the USB3.0 port on the right side of platform

USB2.0 port3



USB charger




Device Control Pins

Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x


Current Limit	MIN	TPY	MAX
TI	2120	2275	2430
PERICOM	2120	2275	2430
NUVOTON	2235	2400	2570

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		USB (USB Charger)	
Title	Document Number		Rev
Size A4	SouthPeak15 TGL		SB
Date: Friday, April 24, 2020		Sheet 36 of 106	Multi


5	4	3	2	1
D				D
C				C
B				B
A				A

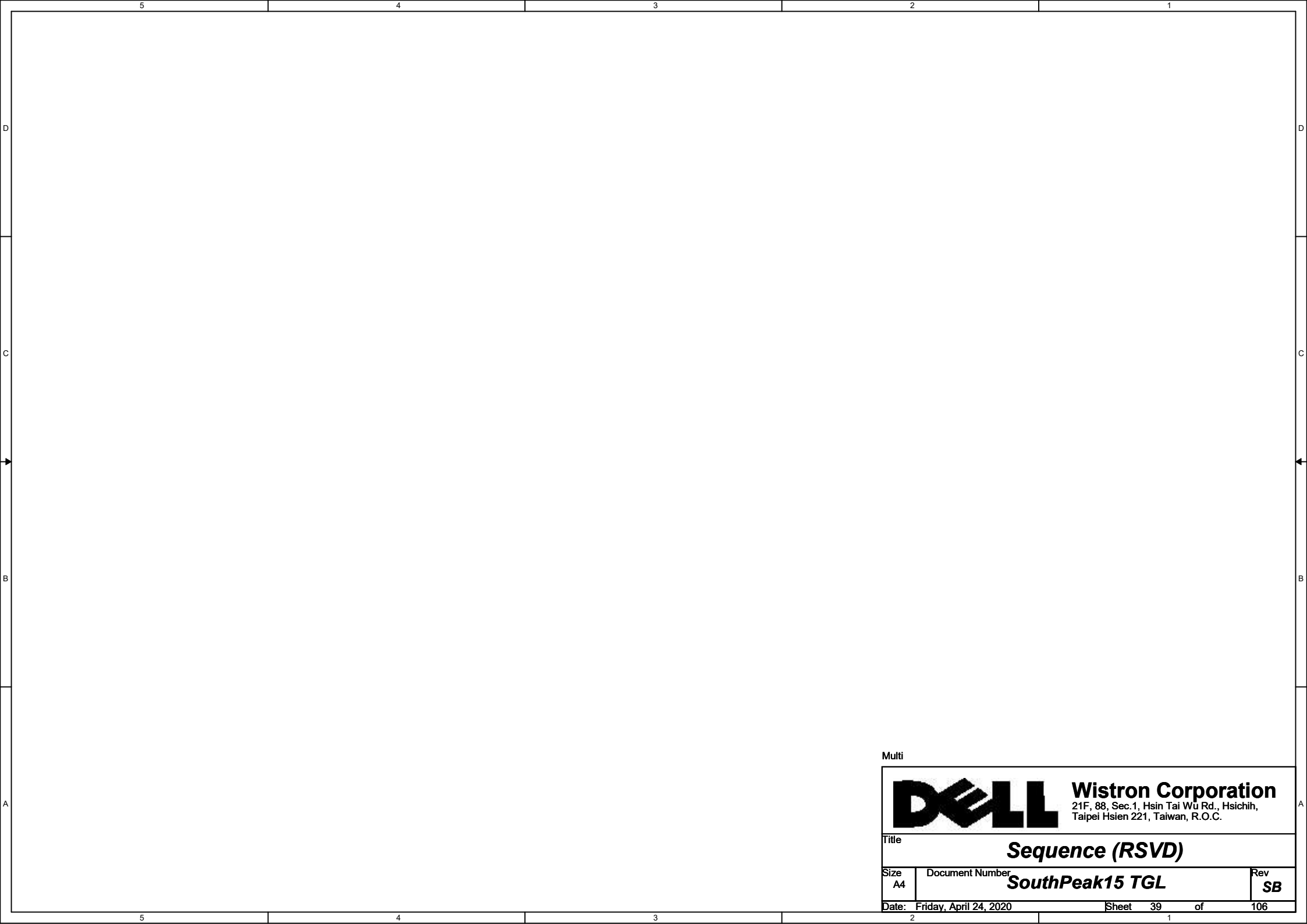
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB (RSVD) (PCIE to USB3.0)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 37	of 106


5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB (RSVD) (USB Redriver/Hub)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 38	of 106



Multi

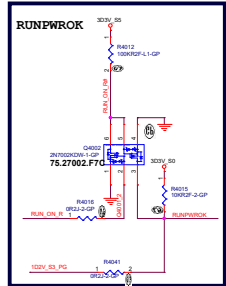
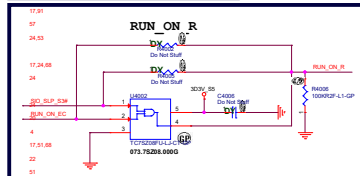
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sequence (RSVD)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 39	of 106

```

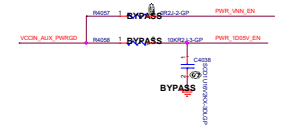
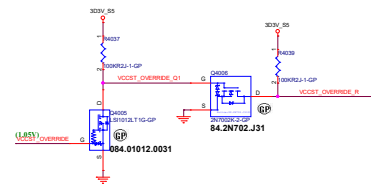
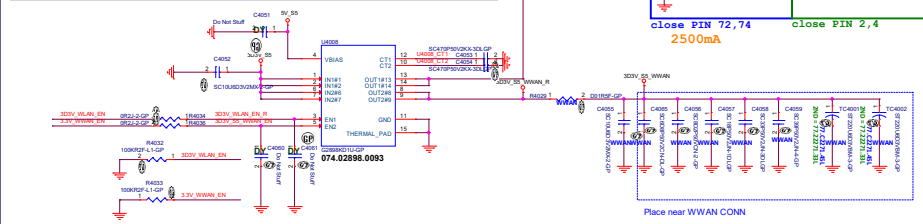
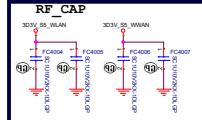
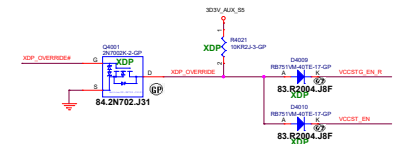
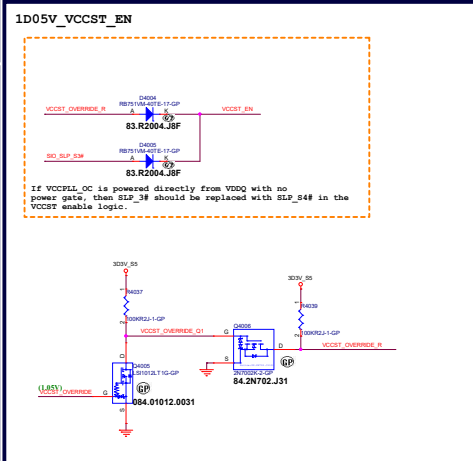
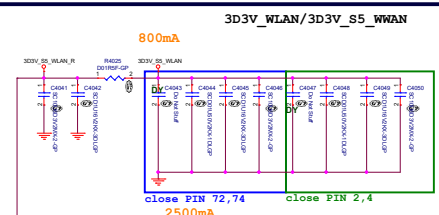
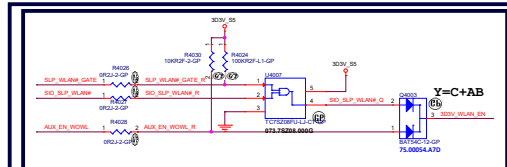
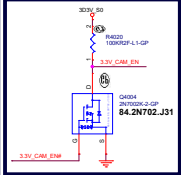
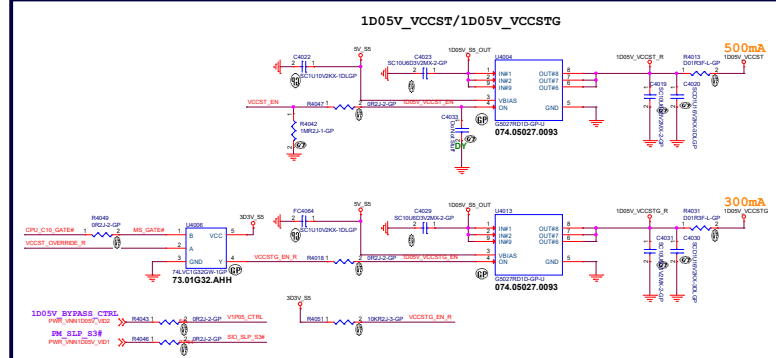
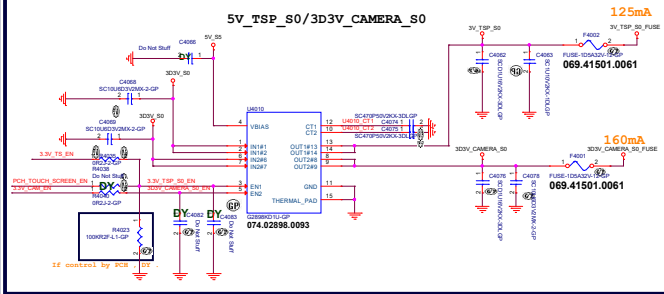
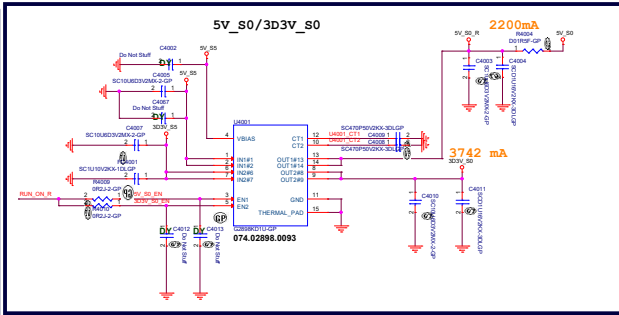
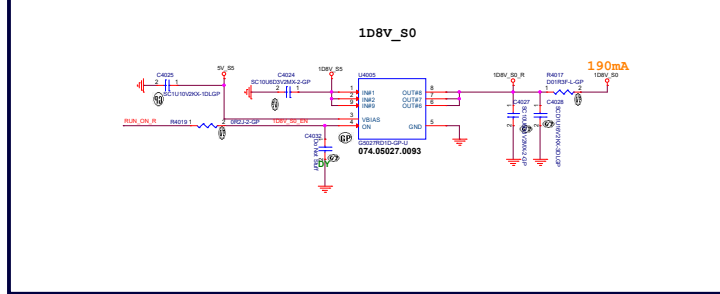
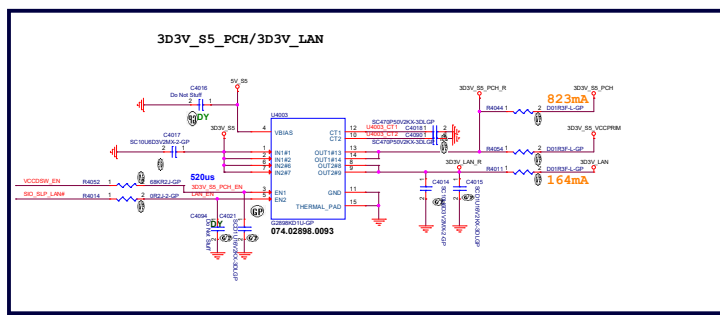
XWLN                                >>>-
3VS3V_SLP                            <<<-
30VS3_PG                             >>>-
5V_PG                                 >>>-
ALW_FWRG2D_3V_3V                    <<<-
SIO_SLP_LANW                         >>>-
SLP_WLAN_GATE                        >>>-
SIO_SLP_WLANW                        >>>-
AUX_EN_WOVL                          >>>-
3_V_WWAN_EN                          >>>-
XCP_OVERRIDEW                        >>>-
CPU_C10_GATEW                        >>>-
RUN_ON_R                               >>>-
VCCDWR_EN                            >>>-

SIO_SLP_S3W                          >>>-
RUN_ON_EC                             >>>-
RUNPWROK                              <<<-
3_V3_TN                               >>>-
TOUCH_SCREEN_EN                      >>>-
3_V3_CAM_EN                           >>>-
SIO_SLP_S4W                           >>>-
VFPDS_CTRL                           <<<-
I2SV_S3_PG                             >>>-
ESP_RESET                             >>>-

```




??? Not ready
Should confirm with Dell




5	4	3	2	1
D				
C				
B				
A				

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Sequence (RSVD) (DS3/S0ix)		
Size A4	Document Number SouthPeak15 TGL	Rev SB
Date: Friday, April 24, 2020		Sheet 41 of 106

5	4	3	2	1
D				D
C				C
B				B
A				A

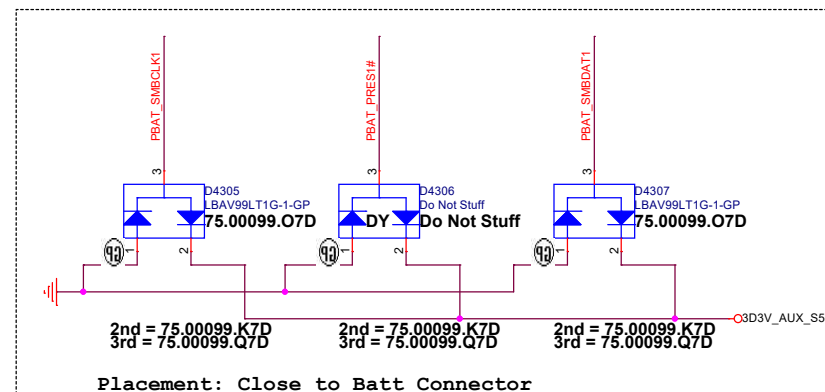
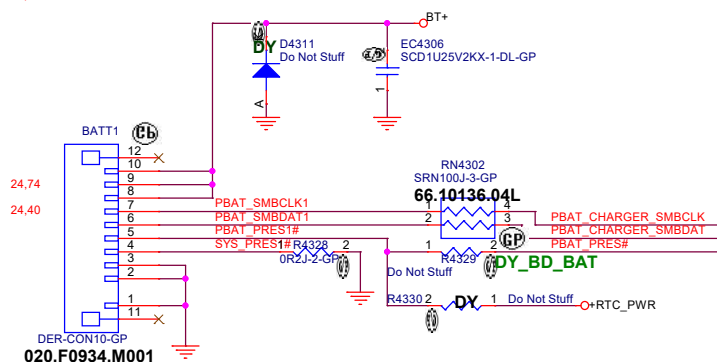
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 42 of	106

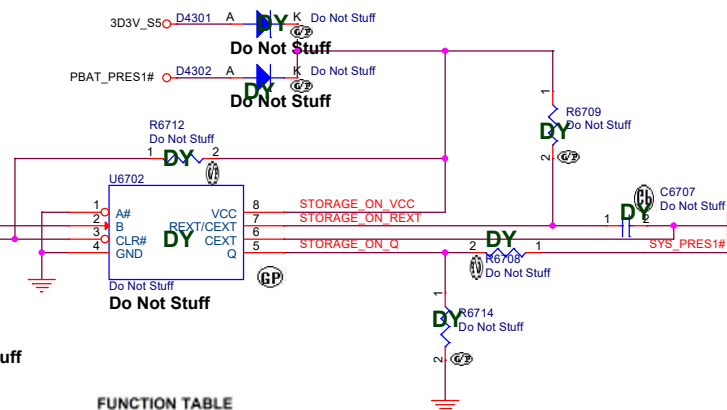
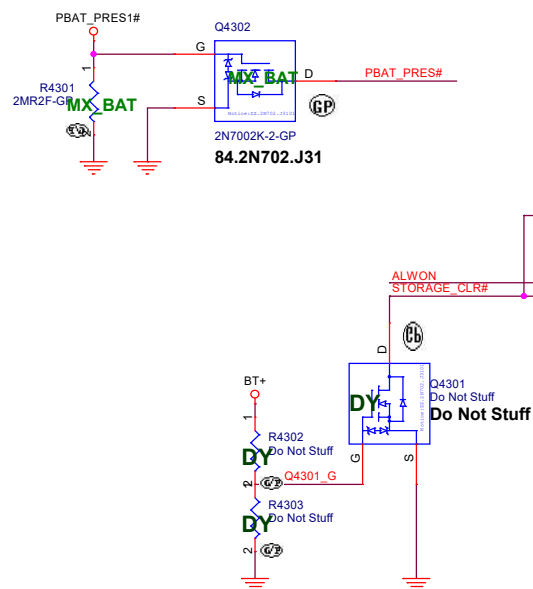
Main Func = BATT Com




	AC_DIS	>>>
	DCIN1_EN	>>>
PBA74_0#	MARGER_SMBCLK	<<>
PBA74_0#	MARGER_SMBDAT	<<>
24.44	PBAT Pres#	<<<
24.44.74	AC_DISC#	<<<
	VBUS2_ECOK	>>>
	ALWON	>>>

Batt Connector



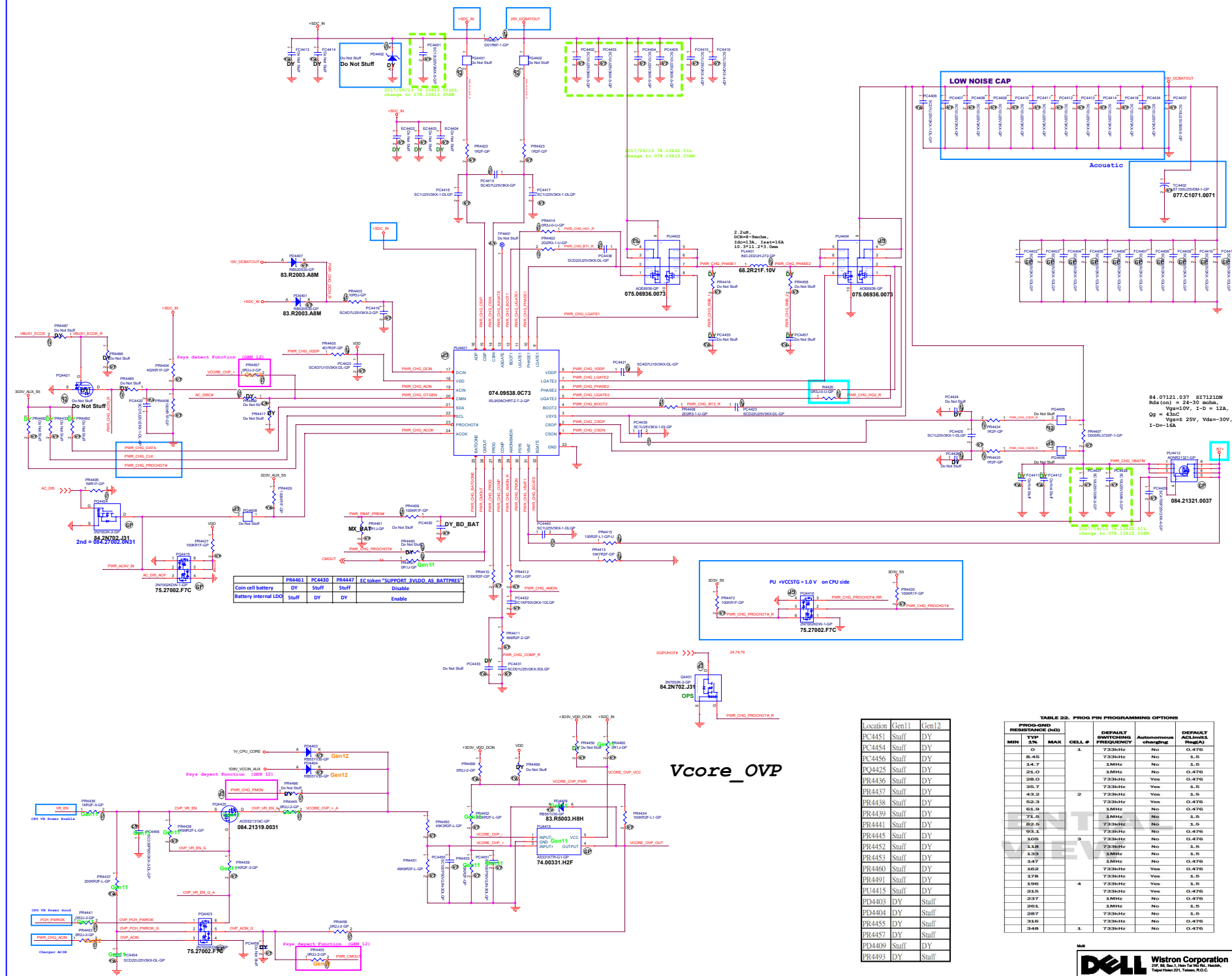
ADVANCED STORAGE MODE



INPUTS			OUTPUTS
A	B	C	Q
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	↑	
H	↓	H	
↑	L	H	

Normal mode

ADVANCED STORAGE MODE Step1.



3.3V 5S

100K01F-GP

PWIR_CHG_PROCHOT#_R

75.27002.FTC

PWIR_CHG_PROCHOT#_RR

3.3V 5S

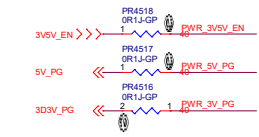
100K01F-GP

PU +VCCSTG = 1.0 V on CPU side

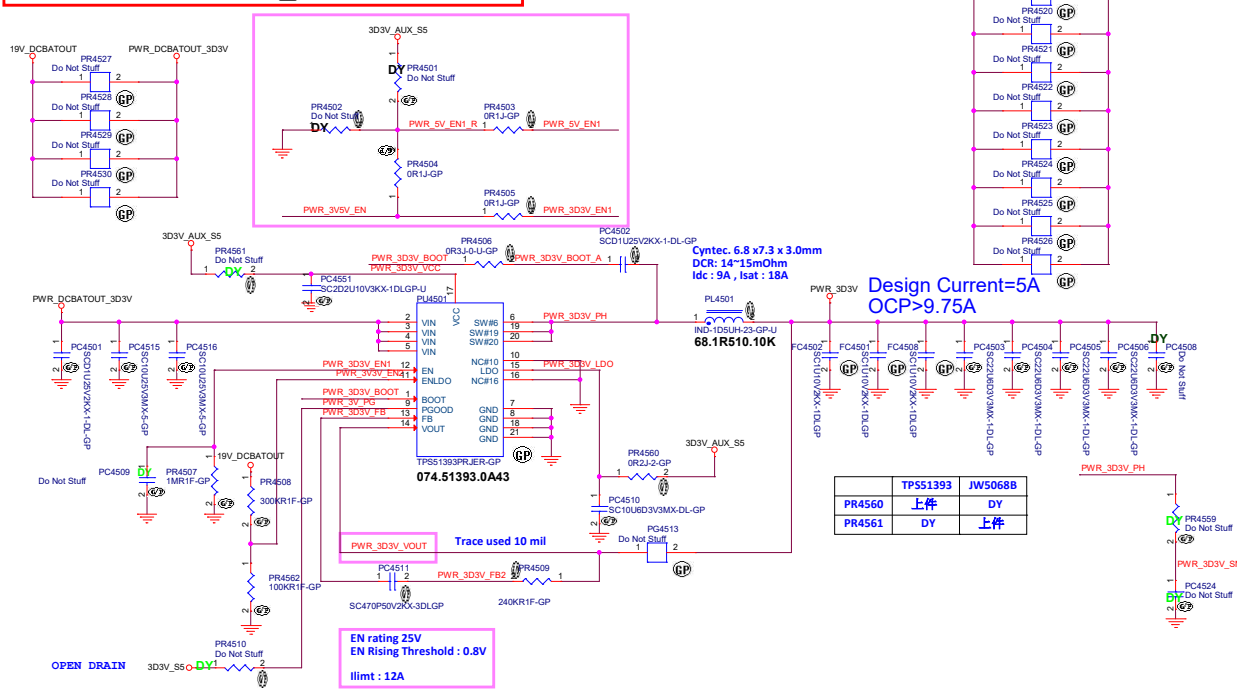
Location	Gen11	Gen12
PC4451	Stuff	DY
PC4454	Stuff	DY
PC4456	Stuff	DY
PC4425	Stuff	DY
PR4436	Stuff	DY
PR4437	Stuff	DY
PR4438	Stuff	DY
PR4439	Stuff	DY
PR4441	Stuff	DY
PR4445	Stuff	DY
PR4452	Stuff	DY
PR4453	Stuff	DY
PR4460	Stuff	DY
PR4491	Stuff	DY
PU4415	Stuff	DY
PD4403	DY	Stuff
PD4404	DY	Stuff
PR4455	DY	Stuff
PR4457	DY	Stuff
PD4409	Stuff	DY
PR4493	DY	Stuff

PROH. PIN RESISTANCE (Ω)		DEFAULT SWITCHING FREQUENCY		DEFAULT Autonomous charging		DEFAULT AClimb15 Resist	
MIN	MAX	TYPE	CELL #	Autonomous	charging	Resist	
9.45	7.33	7.33Hz	No	No	0.47Ω		
14.7	1.0	1.0Hz	No	No	2.5		
28.0	7.33	7.33Hz	No	Yes	0.47Ω		
36.7	7.33	7.33Hz	Yes	Yes	2.5		
52.3	7.33	7.33Hz	Yes	Yes	0.47Ω		
61.0	1.0	1.0Hz	No	No	0.47Ω		
75.5	1.0	1.0Hz	No	No	2.5		
85.0	7.33	7.33Hz	No	No	2.5		
93.3	7.33	7.33Hz	No	No	0.47Ω		
105.6	7.33	7.33Hz	No	No	0.47Ω		
138	7.33	7.33Hz	No	No	2.5		
153	1.0	1.0Hz	No	No	2.5		
162	7.33	7.33Hz	No	No	0.47Ω		
175	7.33	7.33Hz	Yes	Yes	0.47Ω		
215	7.33	7.33Hz	Yes	Yes	2.5		
217	1.0	1.0Hz	No	No	0.47Ω		
261	1.0	1.0Hz	No	No	2.5		
287	7.33	7.33Hz	No	No	2.5		
348	7.33	7.33Hz	No	No	0.47Ω		
386	7.33	7.33Hz	No	No	0.47Ω		

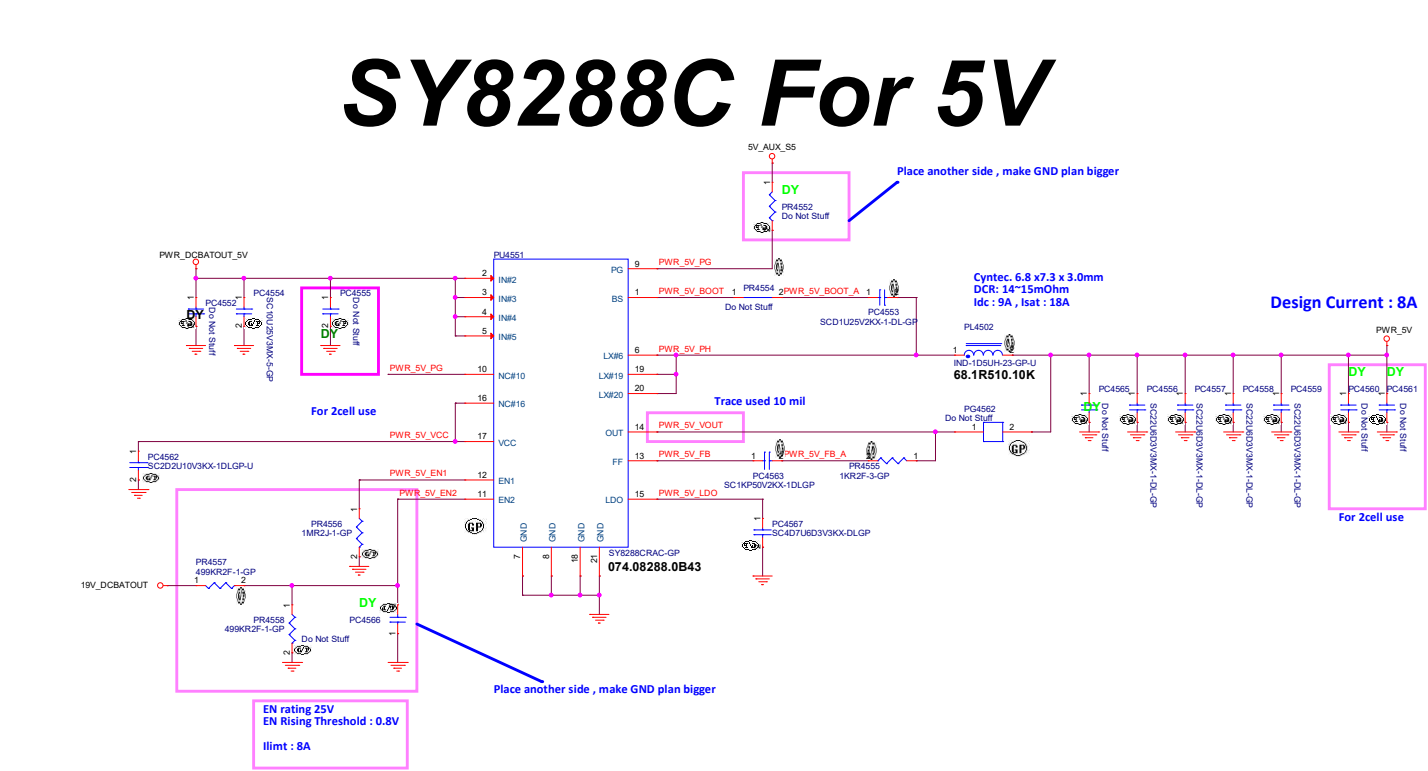
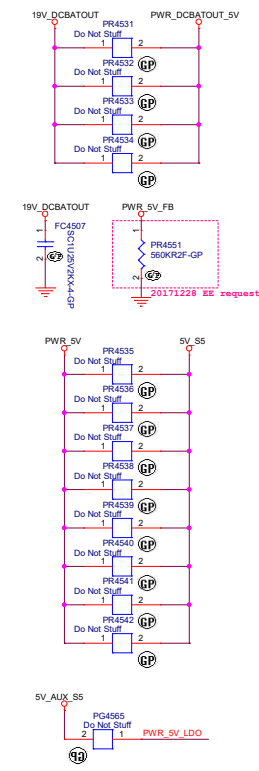
OFFPAGE



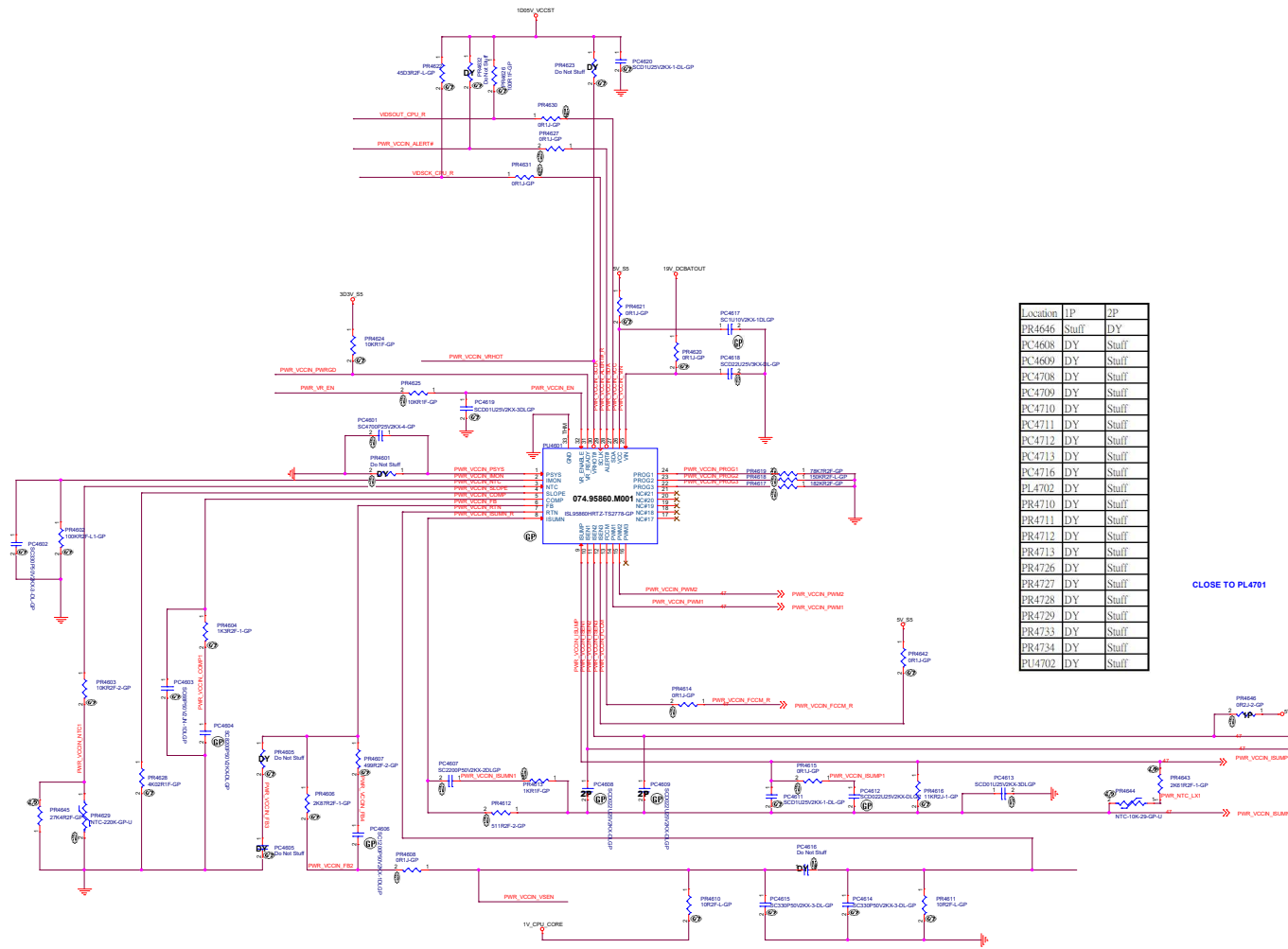
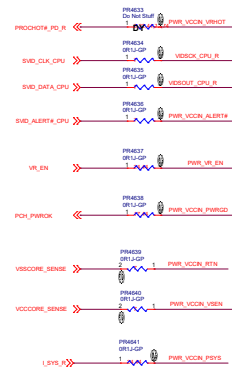
Main Func = Power_System 5V/3D3V



SY8288C For 5V

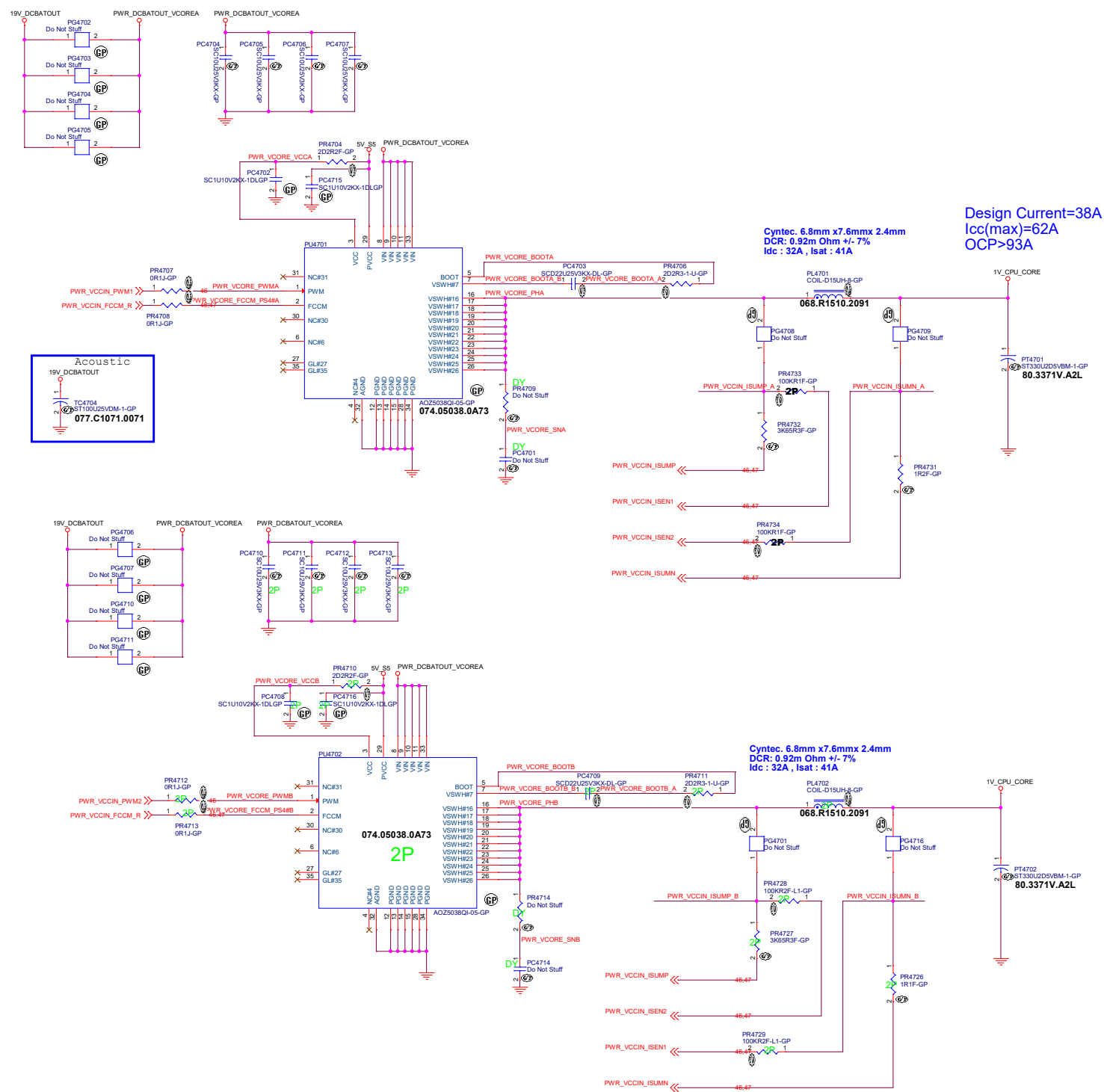


OFFPAGE



Location	1P	2P
PR4646	Stuff	DY
PC4608	DY	Stuff
PC4609	DY	Stuff
PC4708	DY	Stuff
PC4709	DY	Stuff
PC4710	DY	Stuff
PC4711	DY	Stuff
PC4712	DY	Stuff
PC4713	DY	Stuff
PC4716	DY	Stuff
PL4702	DY	Stuff
PR4710	DY	Stuff
PR4711	DY	Stuff
PR4712	DY	Stuff
PR4713	DY	Stuff
PR4726	DY	Stuff
PR4727	DY	Stuff
PR4728	DY	Stuff
PR4729	DY	Stuff
PR4733	DY	Stuff
PR4734	DY	Stuff
PL4702	DY	Stuff

CLOSE TO PL4701



Multi



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu,
Taippei Hsien 221, Taiwan, R.O.C.

Title

Size

A2 Document Number

Rev

SB

Date

Friday, April 28, 2020

Sheet


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of

108


5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title POWER			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 48 of	106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title NCP81210MN_CPU_VCCGTUS		
Size A4	Document Number	Rev SB
Date: Friday, April 24, 2020		Sheet 49 of 106

OFFPAGE

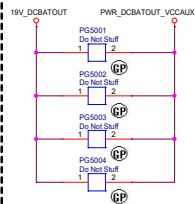
OFFPAGE GAP



PH on CPU side

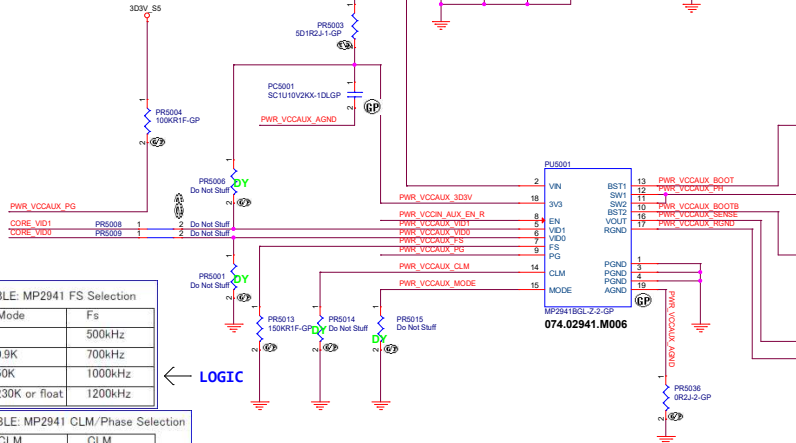


PH on CPU side



VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

LOGIC



RMode	Fs
0	500kHz
90.9K	700kHz
150K	1000kHz
>230K or float	1200kHz

LOGIC

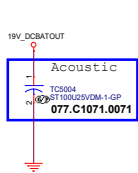
RCLM	CLM
0	7A
90.9K	10A
150K	13A
>230K or float	16A

← LOGIC

RMode	Interleaving	VID Down
0	N	Slew down
90.9K	Y	Slew down
150K	Y	Decay
>230K or float	N	Decay

← LOGIC

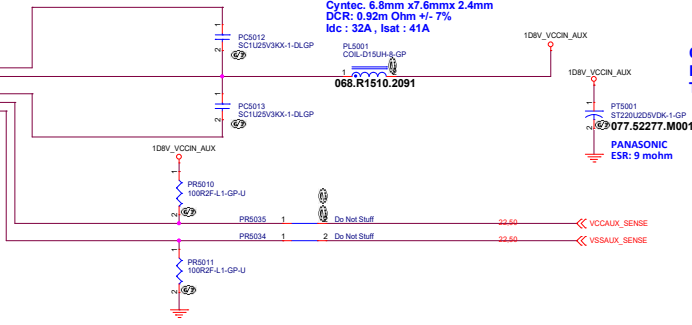
Item	R0 sample	R1 sample
VOUT	1.65V fixed	Defined by VCCPCHCORE_VID1/VID0
RMode	0 ohm	Float
RFS	Float	Float or 150K
1Kohm bleeder	Necessary	Not necessary



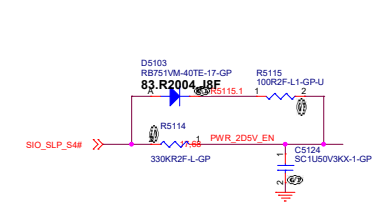
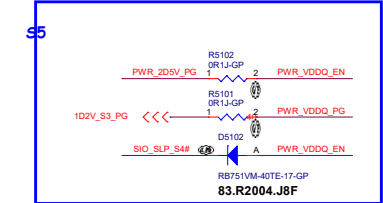
9 Pcs 22uF for 1.0MHz + 5 Pcs 22uF DY

Cyntec. 6.8mm x7.6mmx 2.4mm
DCR: 0.92m Ohm +/- 7%
Idc : 32A , Isat : 41A

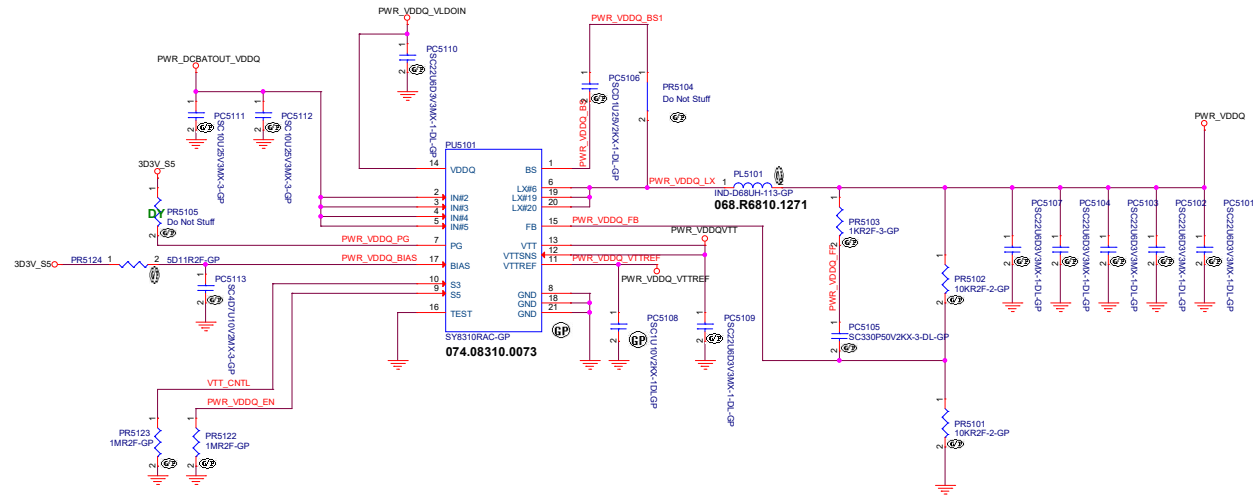
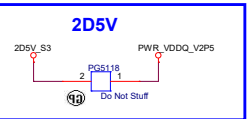
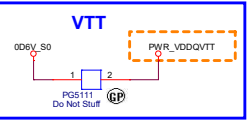
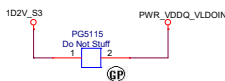
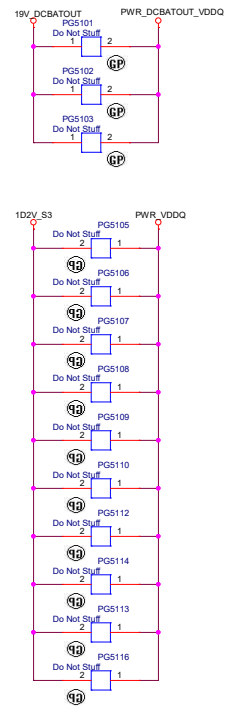
OCP = 40A
Iccmax= 32A
TDC=14A



OFFPAGE



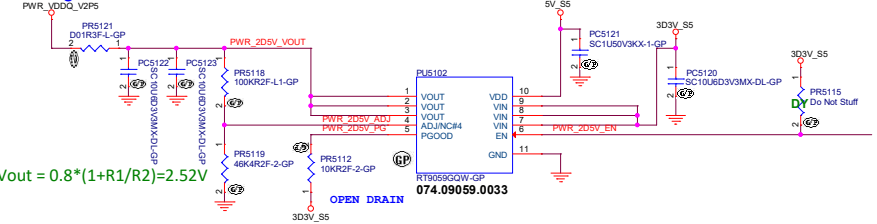
OFFPAGE_GAP



MAX: 300
TPE: 210
Design Current = 0.7A

RT9059GQW for 2D5V

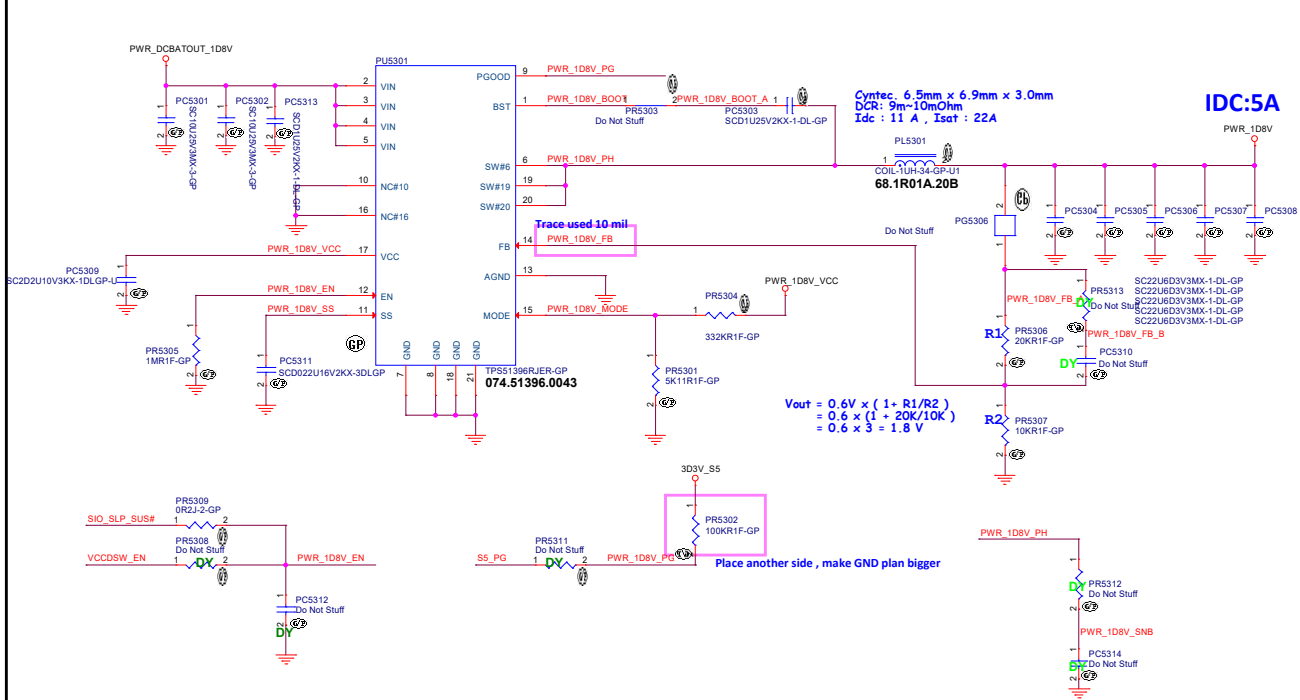
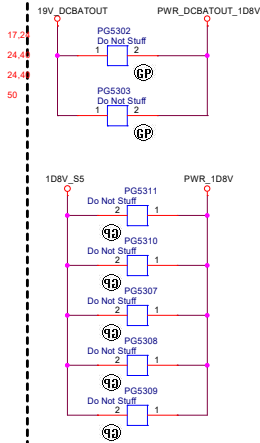
$V_{out} = 0.8 * (1 + R1/R2) = 2.52V$



OFFPAGE-Signal

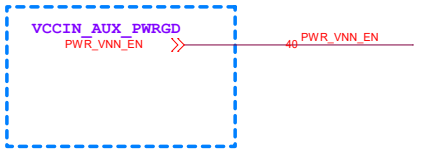
OFFPAGE-GAP

SIO_SLP_SUS# >>>
VCCDSW_EN >>>
SS_PG <<<
PWR_1D8V_PG <<<



OFFPAGE

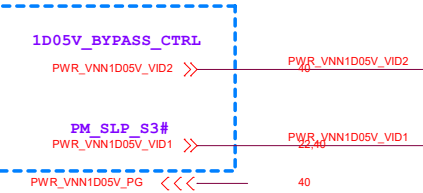
PH on EE Side



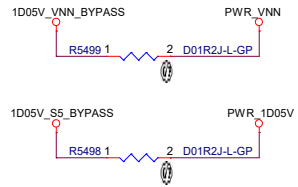
PWR_1D05V_EN

PWR_1D05V_EN

PH on EE Side

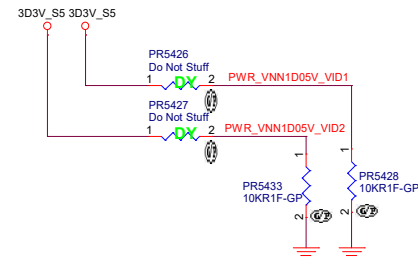
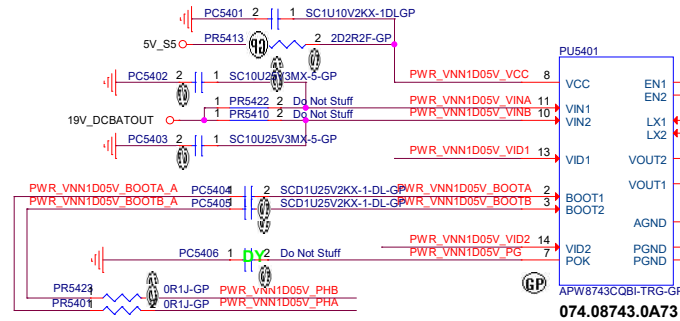
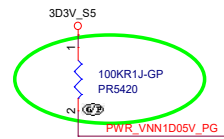


OFFPAGE-GAP



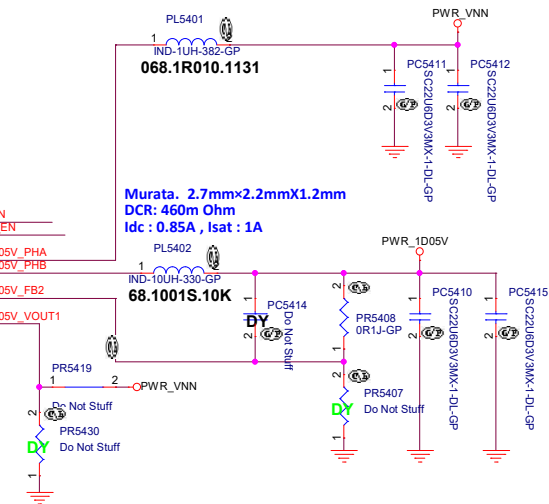
VID1 VNN OUTPUT VOLTAGE	
1	0.78 V
0	1.05 V

VID2 V1P05 OUTPUT VOLTAGE	
1	0.96 V
0	1.05 V



Murata. 2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 3A

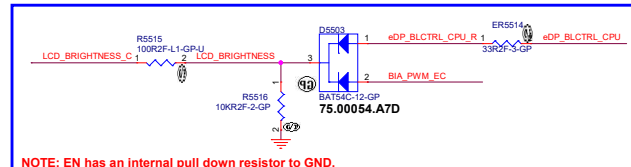
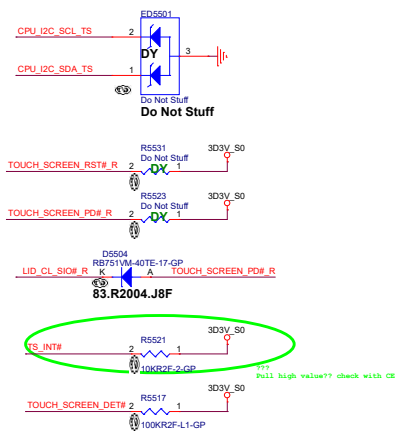
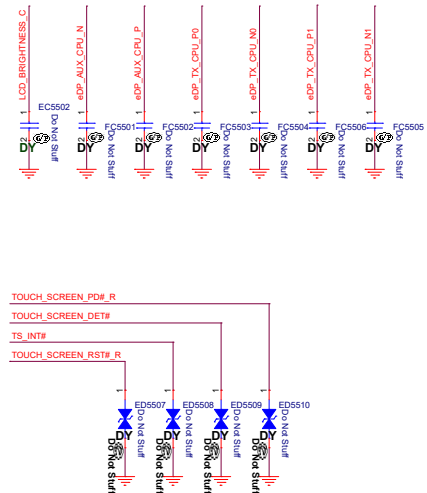
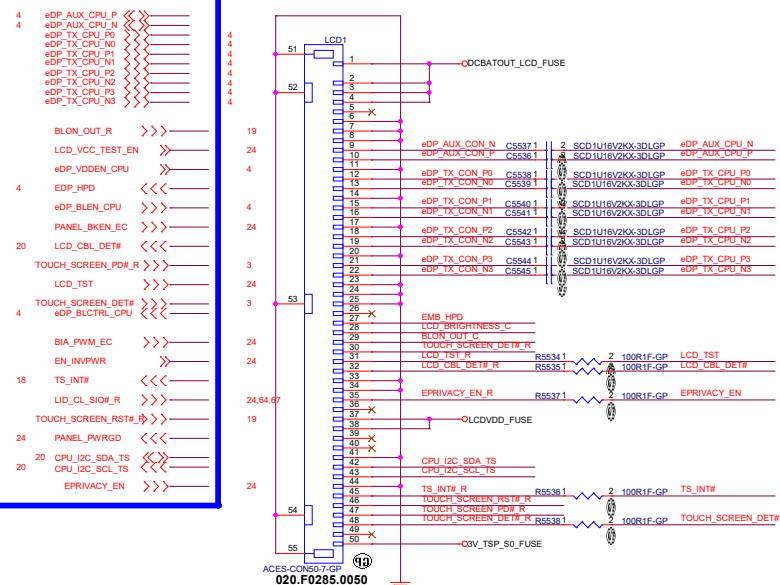
Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A



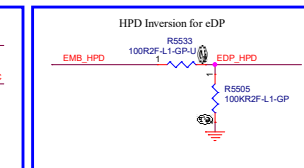
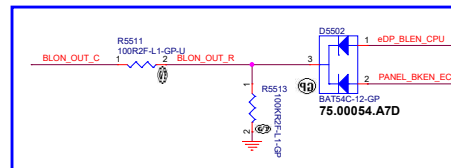
Multi

緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title APW8738_ByPASS	
Size Custom	Document Number SouthPeak15 TGL
Date: Friday, April 24, 2020	Sheet 54 of 106
Rev SB	

Main Func = LCD/Touch

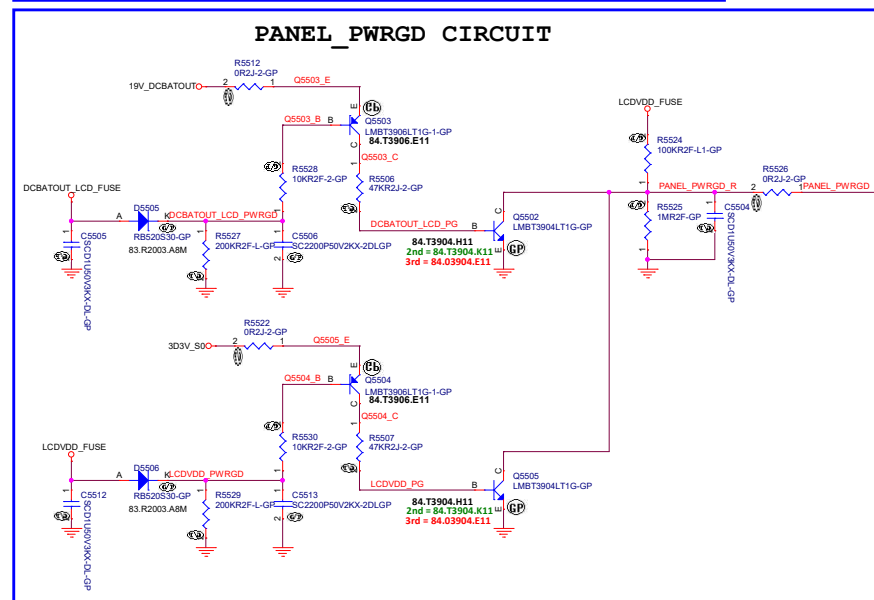
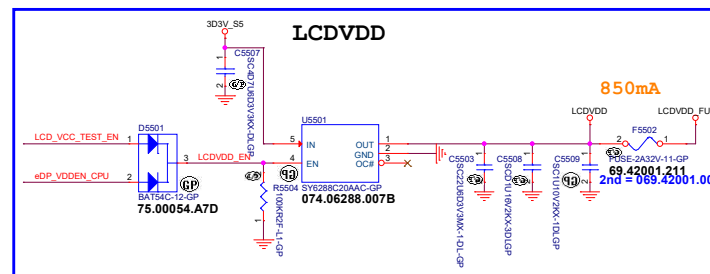
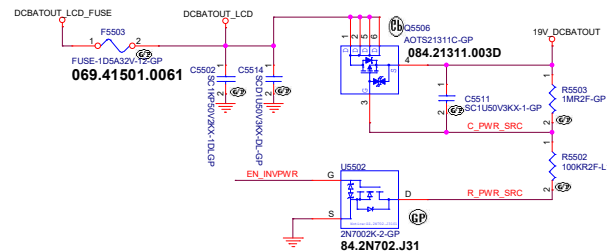


NOTE: EN has an internal pull down resistor to GND



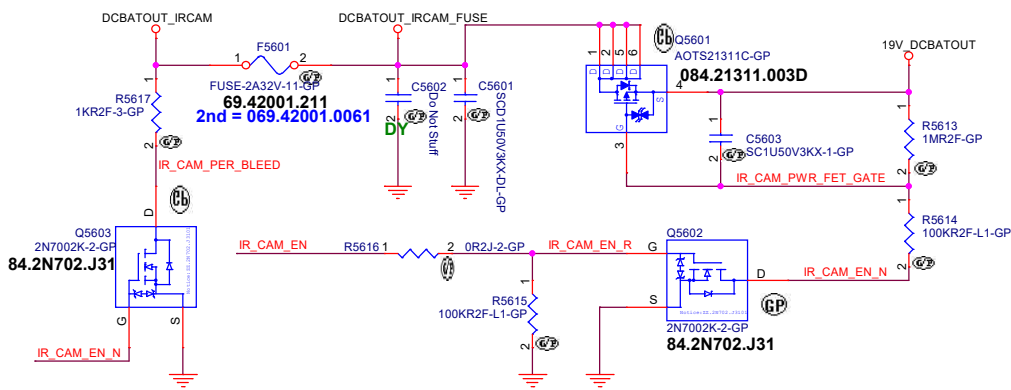
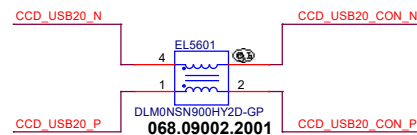
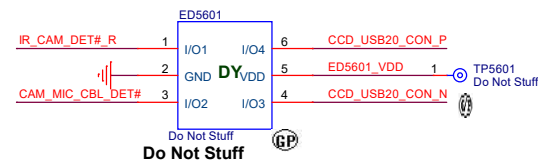
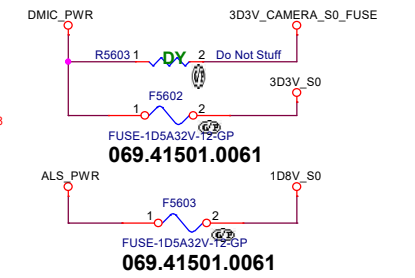
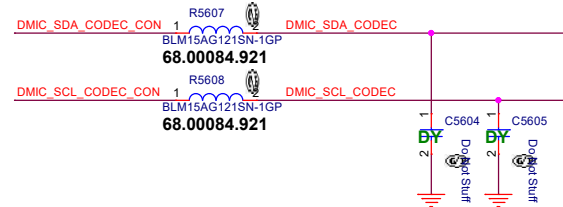
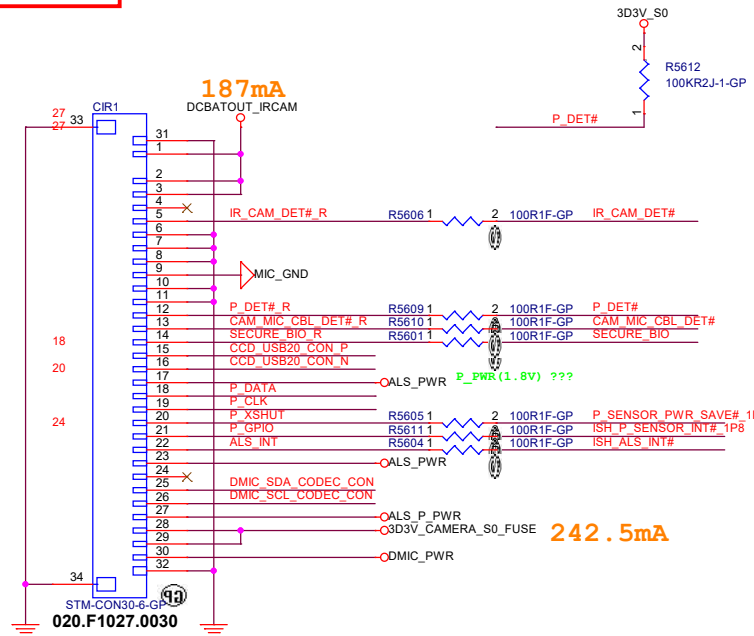
1086mA

INVERTER POWER

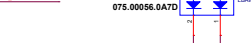
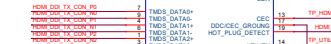
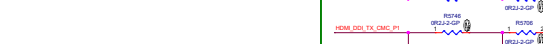


Main Func = IR CAM

OCD_USB20_N <<<>>>
 OCD_USB20_P <<<>>>
 DMIC_SDA_CODECCON <<<>>>
 DMIC_SCL_CODECCON <<<>>>
 20 IR_CAM_DET# <<<>>>
 20 CAM_MIC_CBL_DET# <<<>>>
 P0CLK <<<>>>
 P0DATA <<<>>>
 20 P_DET# <<<>>>
 20 ISH_ALS_INT# <<<>>>
 SECURE_BIO <<<>>>
 P_SENSOR_PWR_SAVE#_1P8 <<<>>>
 20ISH_P_SENSOR_INT#_1P8 <<<>>>
 IR_CAM_EN <<<>>>




	RUN_ON_R	>>>	
	DP2_ODI_TX_P0	>>>	
	DP2_ODI_TX_N0	>>>	
	DP2_ODI_TX_P1	>>>	
	DP2_ODI_TX_N1	>>>	
	DP2_ODI_TX_P2	>>>	
	DP2_ODI_TX_N2	>>>	
	DP2_ODI_TX_P3	>>>	
	DP2_ODI_TX_N3	>>>	
	HDMI_POW	>>>	
4	DP_HPD_CPU	<<<	
4	CPU_DP2_CTRL_CLK	<<<	
4	CPU_DP2_CTRL_DATA	<<<	
24	CSBL	<<<	
24	CSDA	<<<	
24	HDMI_HPD	<<<	




5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Display (RSVD) DP			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 58 of	106


5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Display (RSVD) DVI			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 59 of	106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD)(HDD)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 60 of	106

Main Func = WLAN

WLAN

16 WLAN_PCIE_RX_N
16 WLAN_PCIE_RX_P
16 WLAN_PCIE_TX_N
16 WLAN_PCIE_TX_P

BT

16 BT_USB20_N
16 BT_USB20_P

CNV1

CNV_WR_DN1
CNV_WR_DP1
CNV_WR_DN0
CNV_WR_DP0
CNV_WR_CLKN
CNV_WR_CLKP
CNV_WT_DN1
CNV_WT_DP1
CNV_WT_DN0
CNV_WT_DP0
CNV_WT_CLKN
CNV_WT_CLKP
CNV_BRI_RSP
CNV_RGI_DT
CNV_BRI_DT
CNV_RGI_RSP
CNV_RF_RESET#
CNV_DET#

WLAN

WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
WLAN_CLKREQ_CPU_N

PCIE_WAKE#_R

CNV_COEX3
CNV2_MFUART2_TXD
CNV2_MFUART2_RXD

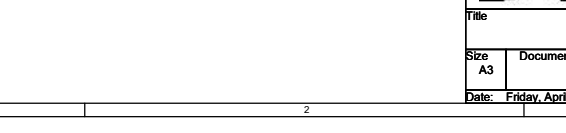
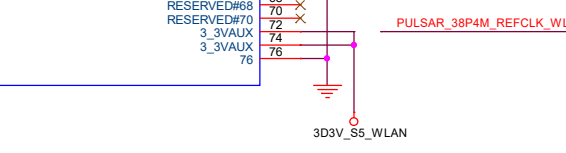
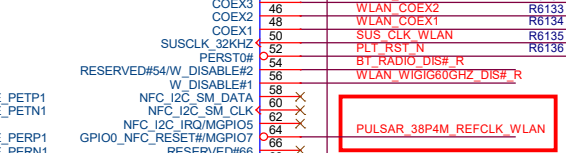
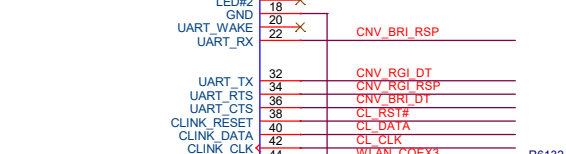
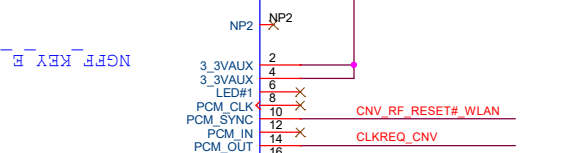
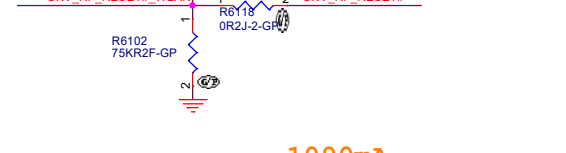
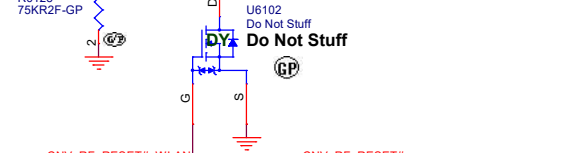
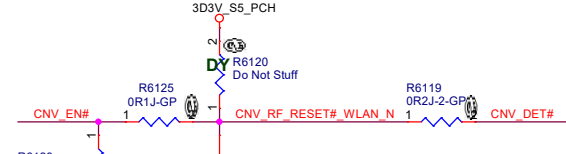
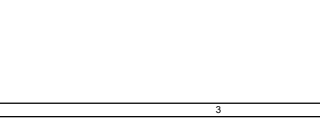
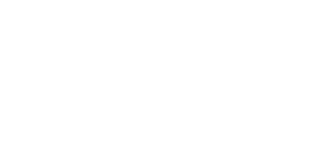
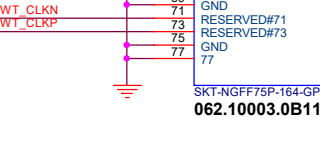
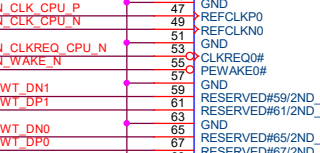
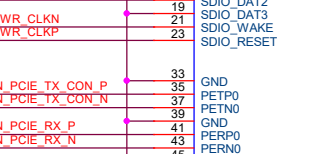
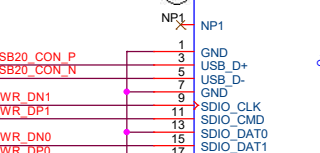
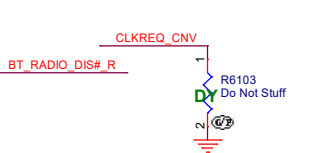
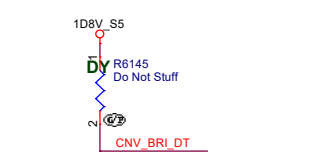
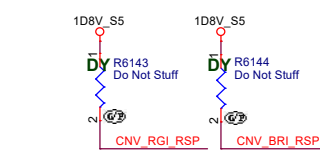
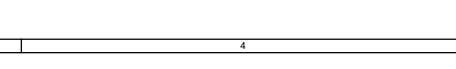
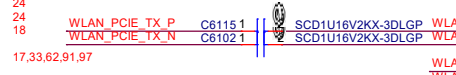
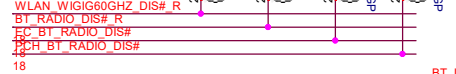
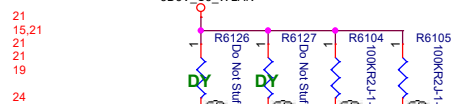
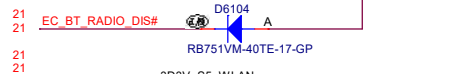
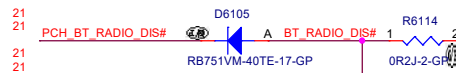
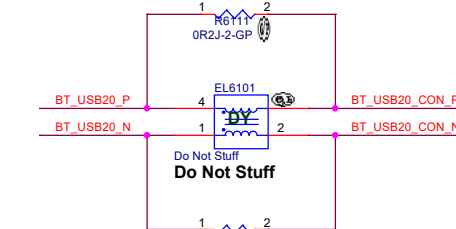
CLK_CLK
CLK_DATA
CLK_RST#

CLKREQ_CNV
WLAN_WIGIG60GHZ_DIS#
EC_BT_RADIO_DIS#
SUSCLK

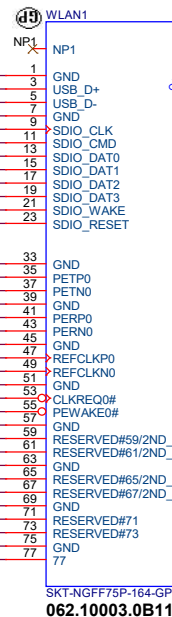
PCH_PLTRST#_RIGHT

CNV_EN#

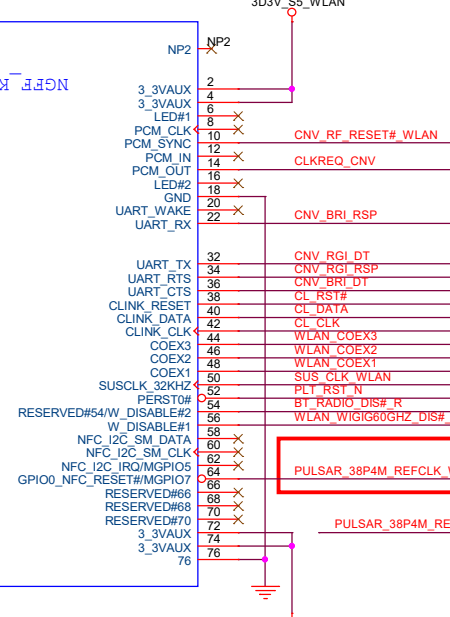
PCH_BT_RADIO_DIS#



1090mA



NGFF_KEY_E_75P



PULSAR_38P4M_REFCLK_WLAN

Multi



INT IO (WLAN M.2)

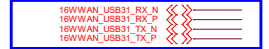
Size A3 Document Number Rev SB

Date: Friday, April 24, 2020 Sheet 61 of 106

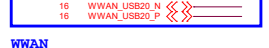
Main Func = WWAN

NGFF(WWAN/SSD)

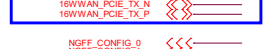
WWAN



WWAN



WWAN



NGFF_CONFIG_0, NGFF_CONFIG_1, NGFF_CONFIG_2, NGFF_CONFIG_3



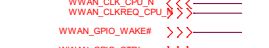
WWAN_RADIO_DIS#, GPS_DISABLE#



20CPU_I2C_SDA_GNSS, 20CPU_I2C_SCL_GNSS, PCH_PLTRST#_RIGHT



PCIE_WAKE#_R



CNV_COEX3, 20BVB_MFUART2_TXD, 20BVB_MFUART2_RXD



WWAN_CLK_CPU_P, WWAN_CLK_CPU_N, WWAN_CLKREG_CPU#



WWAN_GPIO_WAKE#



WWAN_GPIO_CTRL#



WWAN_BB_RST#



PCH_PCIE_WAKE#



SAR_DRP#



SSD_SCP#



WWAN_FULL_PWR_EN_R



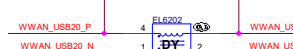
WWAN_RADIO_DIS#, WWAN_RADIO_DIS#_R



GPS_DISABLE#, GPS_DISABLE#_R



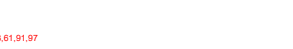
WWAN_USB20_P, WWAN_USB20_CON_P



WWAN_USB20_N, WWAN_USB20_CON_N



Do Not Stuff, Do Not Stuff



NGFF_CONFIG_2, NGFF_CONFIG_2_R



NGFF_CONFIG_1, NGFF_CONFIG_1_R



WWAN_BB_RST#, WWAN_BB_RST#_R



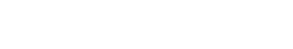
WWAN_PCIE_TX_P, WWAN_PCIE_TX_CON_P



WWAN_PCIE_TX_N, WWAN_PCIE_TX_CON_N



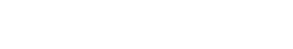
WWAN_PCIE_RX_P, WWAN_PCIE_RX_CON_P



WWAN_PCIE_RX_N, WWAN_PCIE_RX_CON_N



WWAN_USB31_TX_P, WWAN_USB31_TX_CON_P



WWAN_USB31_TX_N, WWAN_USB31_TX_CON_N



WWAN_USB31_RX_P, WWAN_USB31_RX_CON_P



WWAN_USB31_RX_N, WWAN_USB31_RX_CON_N



SAR_DRP#, SAR_DRP#_R



NGFF_CONFIG_0, NGFF_CONFIG_0_R

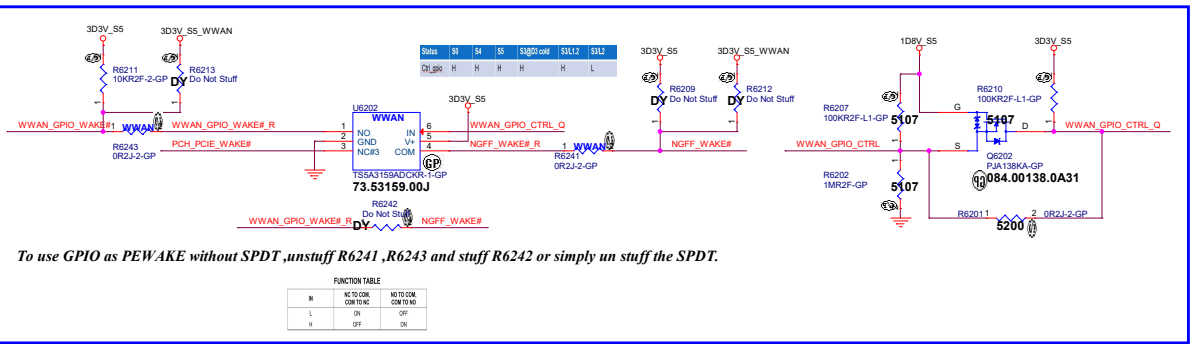


NGFF_CONFIG_3, NGFF_CONFIG_3_R



2500mA

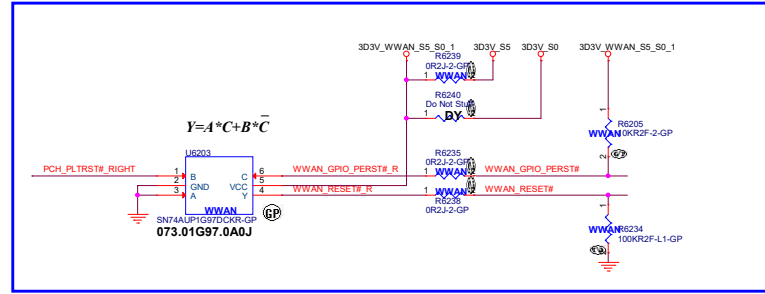
062.10003.0221



To use GPIO as PEWAKE without SPDT, unstuff R6241, R6243 and stuff R6242 or simply un stuff the SPDT.

FUNCTION TABLE

N	NO TO COM	COM TO NO
H	ON	OFF
L	OFF	ON



STATE #

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	WWAN_PCIE_TX/SSD
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIe(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIe(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN-USB3.1, PCIe Gen1	0

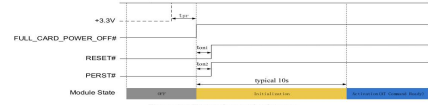


Figure 3-5 Timing Control for Start-up

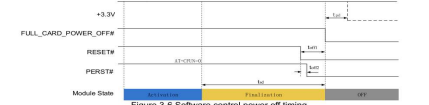
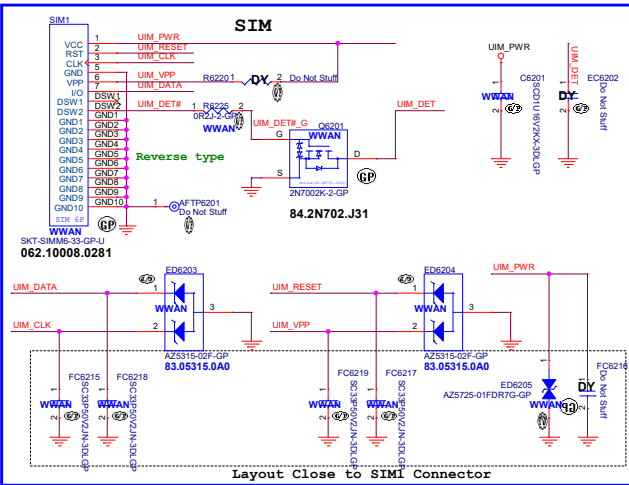


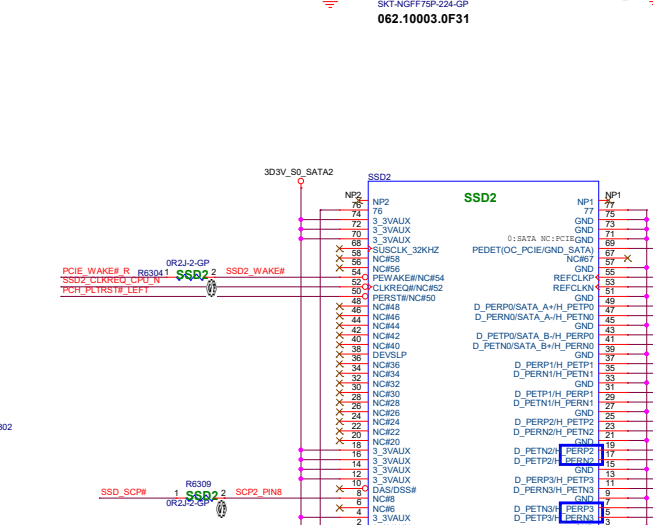
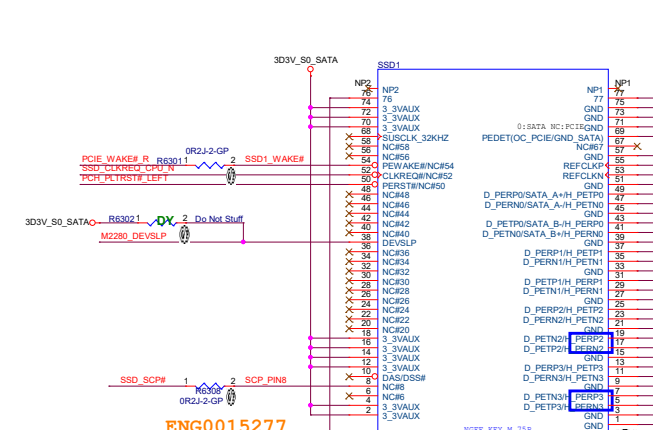
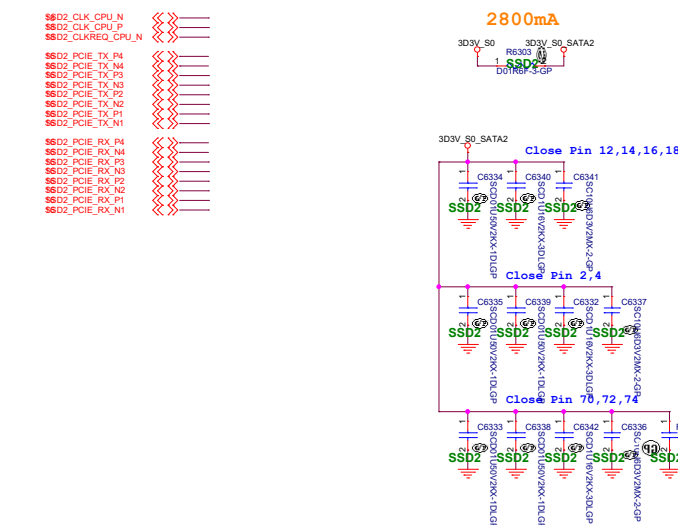
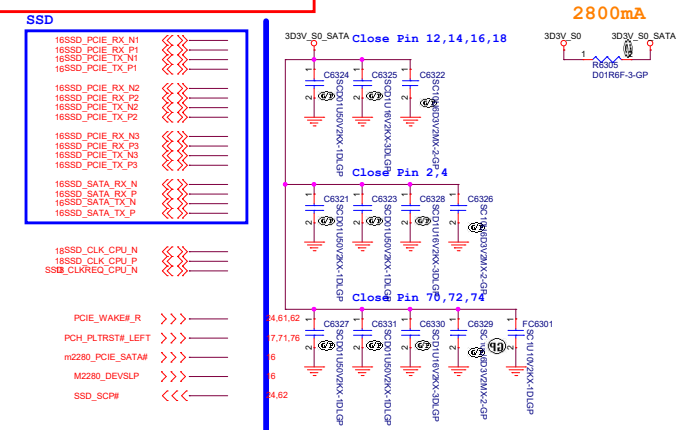
Figure 3-6 Software control power off timing

Index	Minimum	Typical	Notes
t _{SP}	-	-	+3.3V power supply rises time. If power supply always ready, there is no t _{SP} .
t _{on1}	10ms	30ms	If the RESET# has a residual voltage, then 30ms is necessary
t _{on2}	10ms	30ms	PERST# should be asserted after FULL_CARD_POWER_OFF#



Layout Close to SIM Connector

Main Func = m.2 SSD



PEDET	0	Host I/F Indication; To be grounded for SATA, No Connect for PCIe	0V
-------	---	--	----

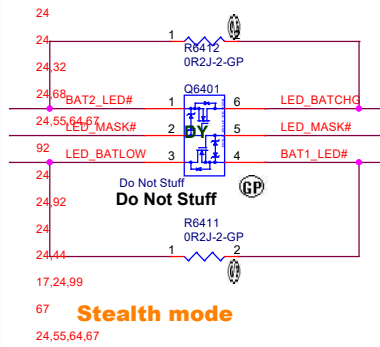
L	SATA
H	PCIe

74	3.3V	GN0	75
72	N/C	GN3	73
70	3.3V	GN6	71
68	SUSCLK (20MHz) (I/O) (3.3V)	PEDET (NC-PCIE/GMIO-SATA)	67
	Connector Key	N/C	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GN0	57
54	N/C	REFCLK	55
52	PEWAKE (I/O) (3.3V) or N/C	REFCLK	53
50	CLKREQ (I/O) (3.3V) or N/C	GN1	51
48	PERST (I/O) (3.3V) or N/C	PETp/SATA-A+	49
46	N/C	PETp/SATA-A-	47
44	N/C	GN2	45
42	N/C	PERPp/SATA-B-	43
40	N/C	PERPp/SATA-B+	41
38	DEVSLP (O)	GN2	39
36	N/C	PETp-1	37
34	N/C	PETp-1	35
32	N/C	GN3	33
30	N/C	PERp-1	31
28	N/C	PERp-1	29
26	N/C	GN2	27
24	N/C	PETp-2	25
22	N/C	PETp-2	23
20	N/C	GN2	21
18	3.3V	PERp-2	19
16	3.3V	PERp-2	17
14	3.3V	PETp-3	15
12	N/C	PETp-3	13
10	DAS/DSS# (I/O) (LED1#) (I/O) (3.3V)	PETp-3	11
8	N/C	GN0	9
6	N/C	PERp-3	7
4	N/C	PERp-3	5
2	3.3V	GN0	3
		GN2	1

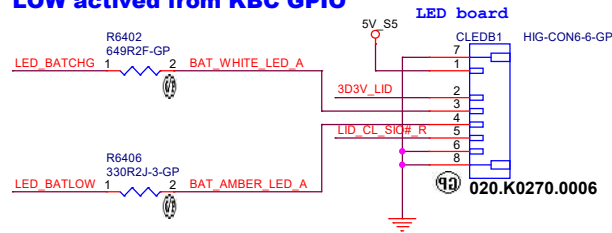
Multi	
 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wai Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (SSD M.2/ eMMC)	
Size A2	Document Number Rev SB

Main Func = LED/HALL/Button

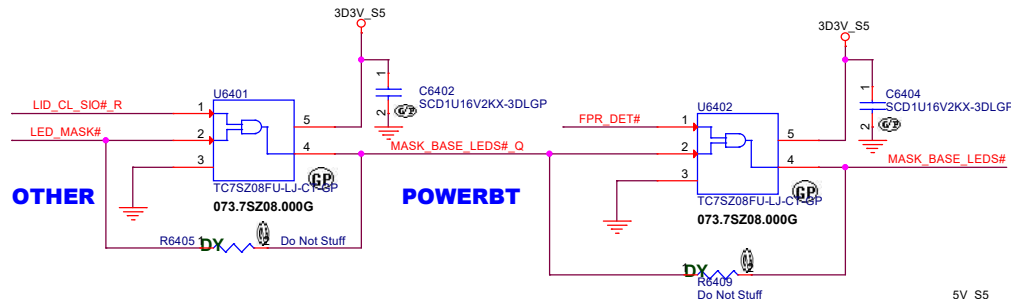
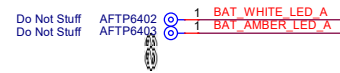
BAT2_LED# >>>
 BAT1_LED# >>>
 LED_MASK# >>>
 KBC_PWRBTN# <<<
 LID_CL_SIO#_R <<<
 MASK_BASE_LEDS#_Q <<<
 BREATH_LED# <<<
 FPR_DET# >>>
 M_BIST >>>
 ACAV_IN >>>
 RSMRST#_KBC >>>
 3D3V_LID >>>
 LID_CL_SIO#_R >>>



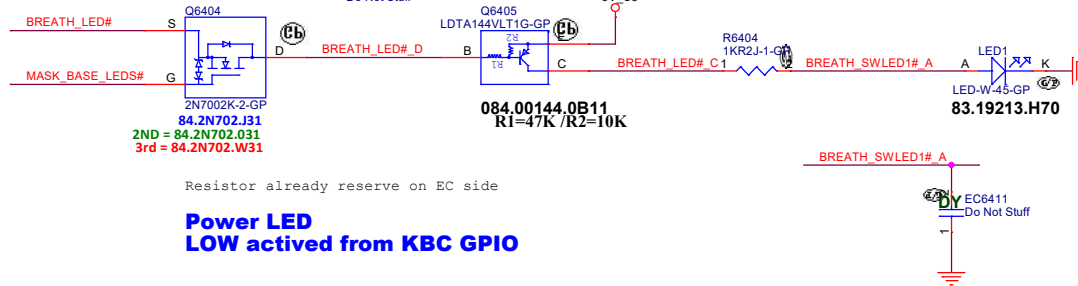
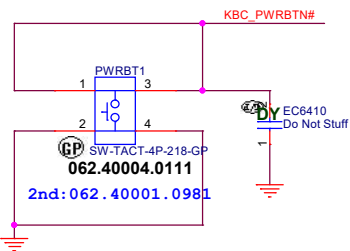
Battery LED2(White LED) LOW acted from KBC GPIO



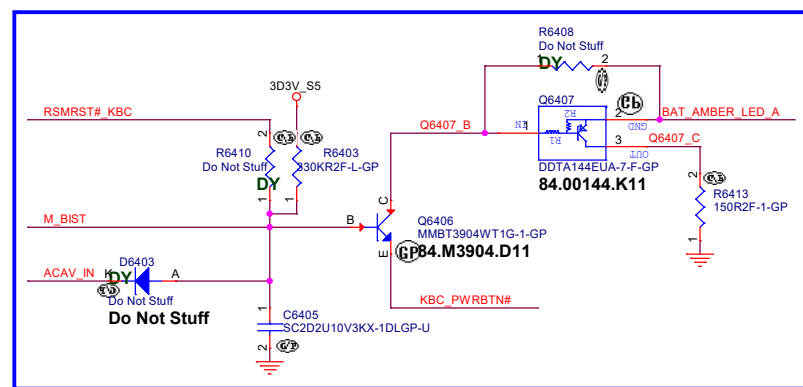
Battery LED1(Orange LED) LOW acted from KBC GPIO



POWER BUTTON



M-BIST



Multi

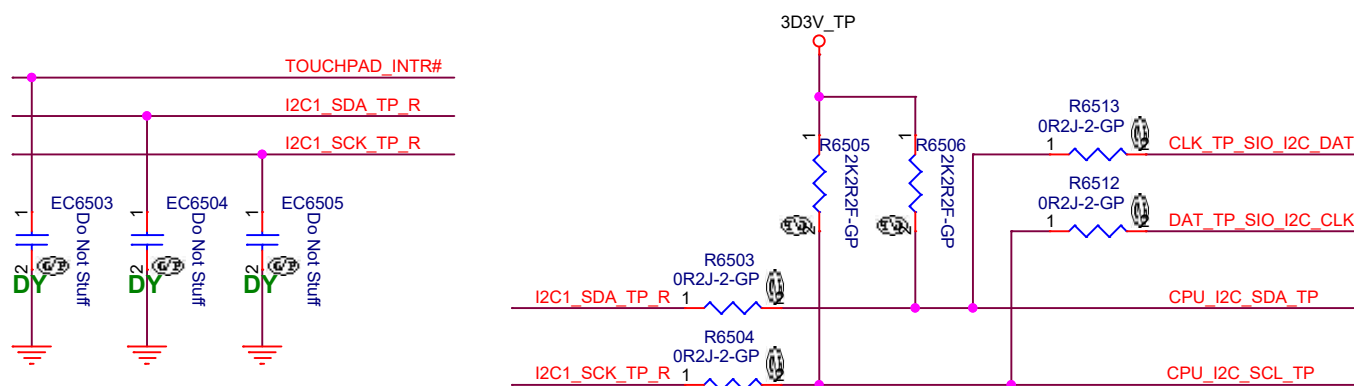
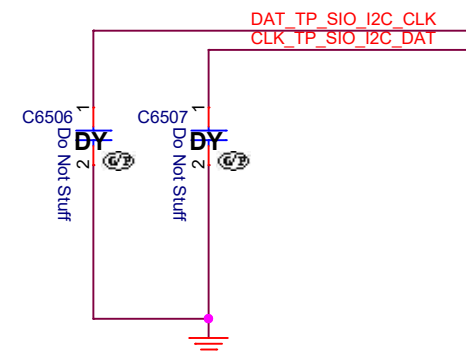
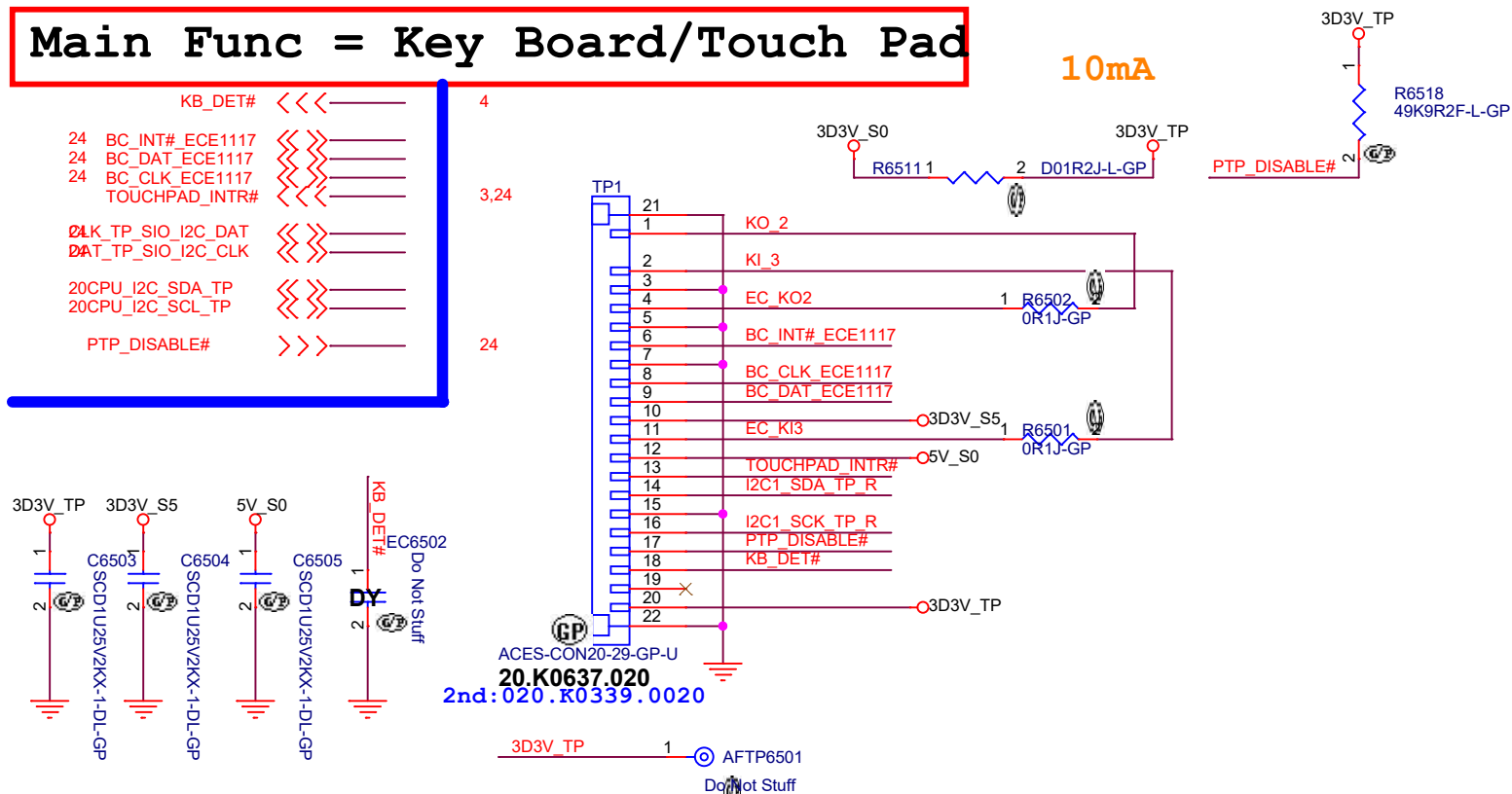


Title LED / Button / Power Button

Size Custom Document Number Rev SB

Date: Friday, April 24, 2020 Sheet 64 of 106

Main Func = Key Board/Touch Pad



Multi



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Title

INT IO (KB/TP)

Size	A4
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Document Number

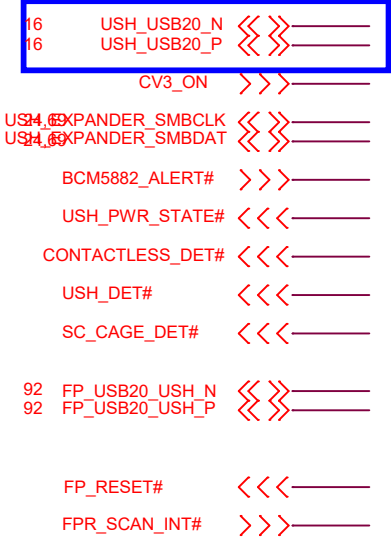
Rev
SE

Date: Friday, April 24, 2020

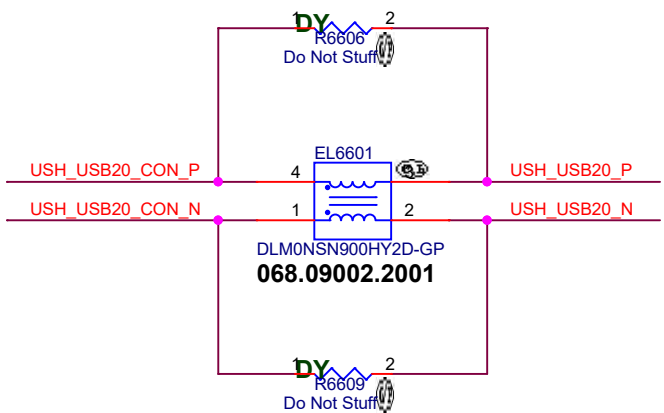
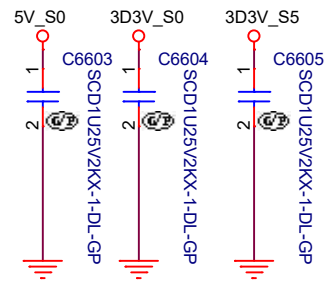
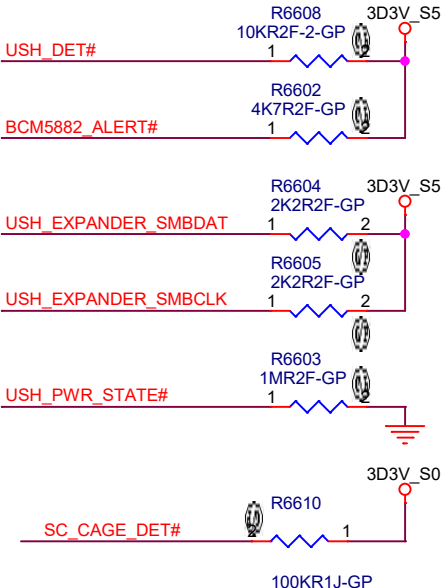
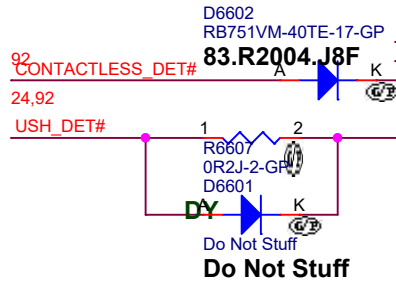
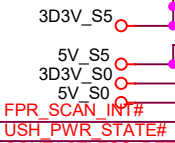
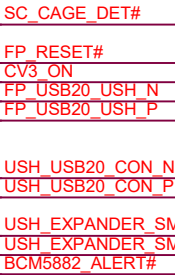
Sheet 65 of 106

Main Func = USH BD


USH



CV3 module	
pin assignment -proposal 2	
NC	
NC	
CV2_ON	
USB20_N from FPR	
USB20_P from FPR	
GND	
GND	
USB20_N to PCH	
USB20_P to PCH	
GND	
USH_EXPANDER_SMBCLK	
USH_EXPANDER_SMBDAT	
BCM5882_ALERT#	
+3.3V_ALW	
+3.3V_ALW	
+3.3V_ALW	
+3.3V_ALW	
+3.3V_RUN	
+3.3V_RUN	
USH_RST#	
USH_PWR_STATE#	
CONTACTLESS_DET#	
GND	
GND	
USH_DET#	



Multi



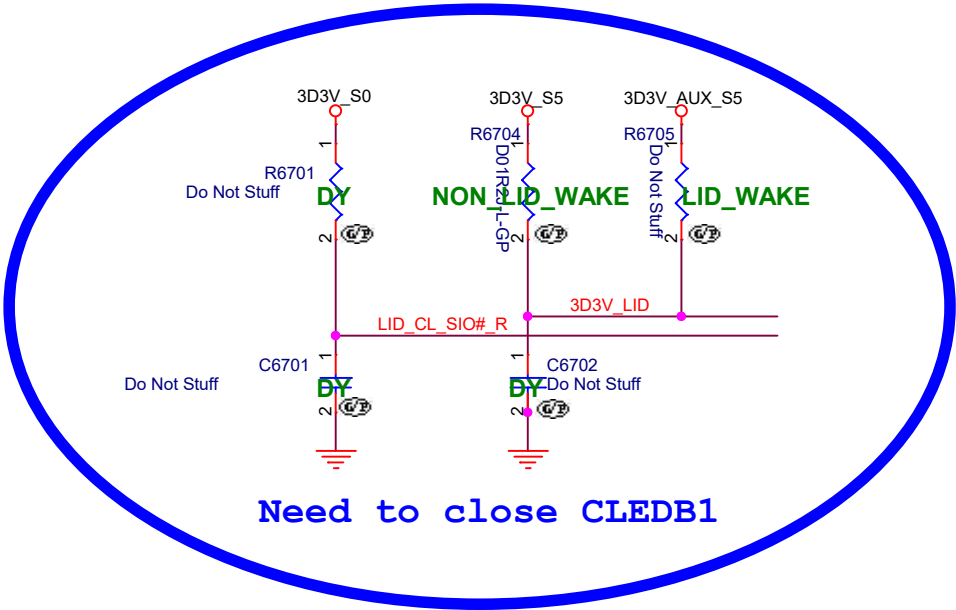
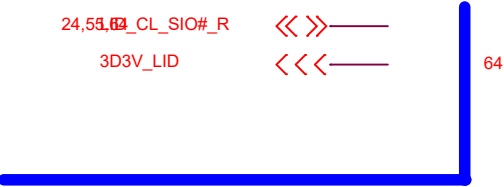
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Title
IO Board Conn (USH)


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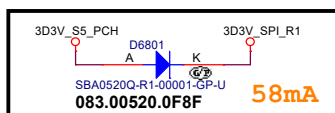
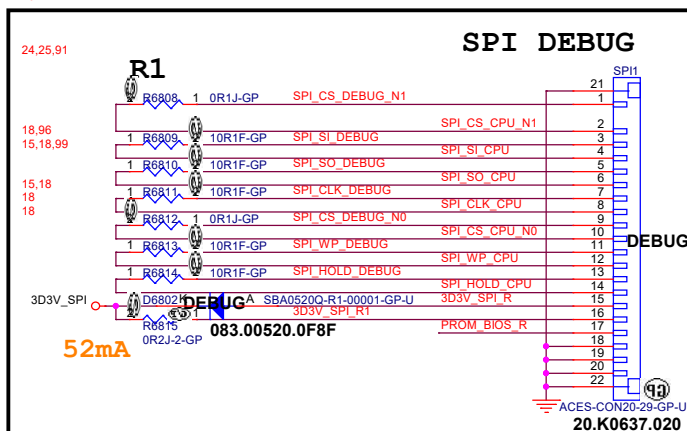
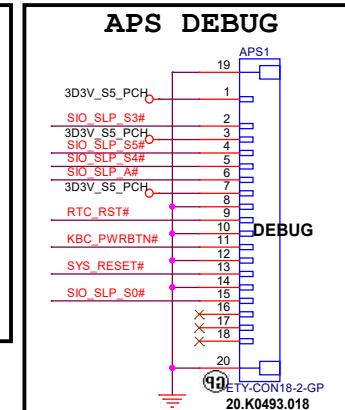
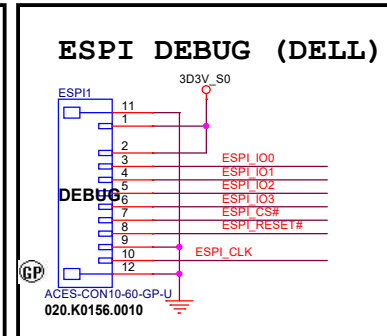
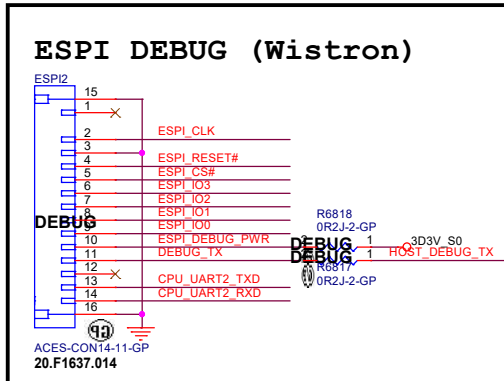
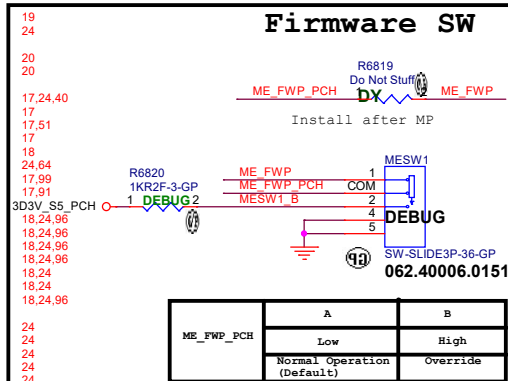
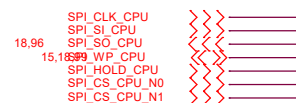
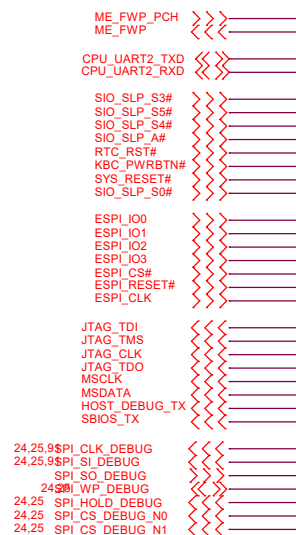
Main Func = Sensor (Hall-Sensor)



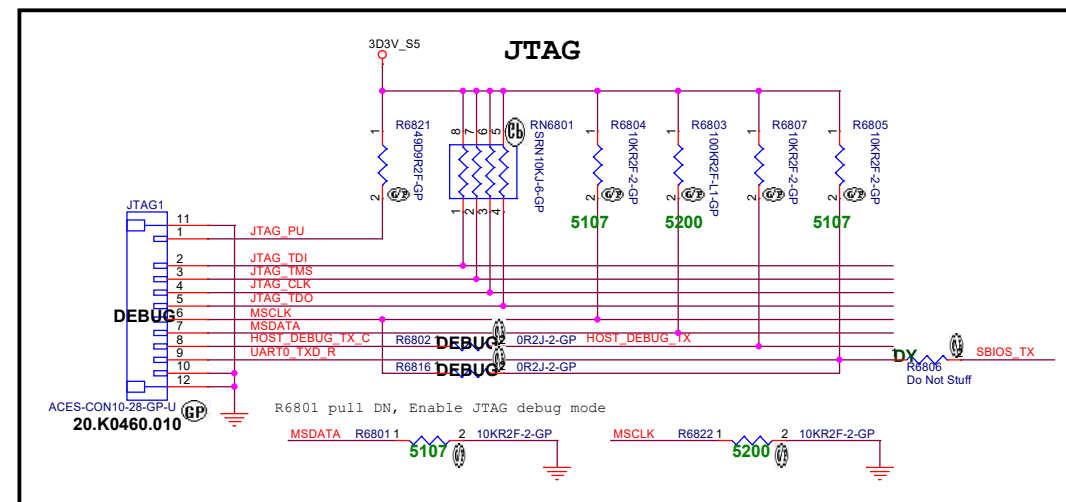
Multi

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Title Sensor (Hall-Sensor)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 67 of	106

Main Func = Debug

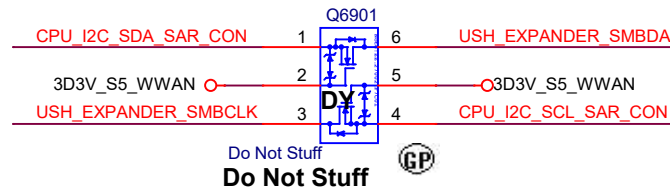
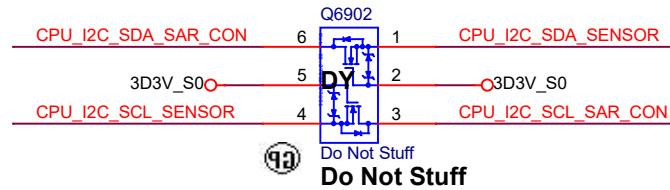
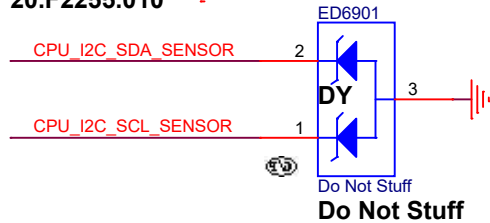
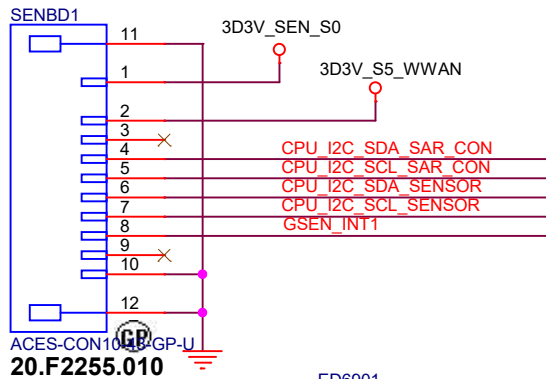
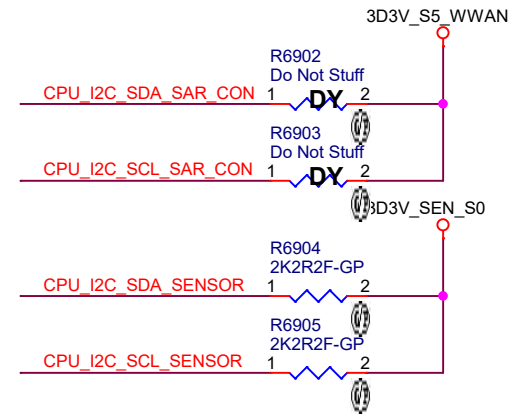
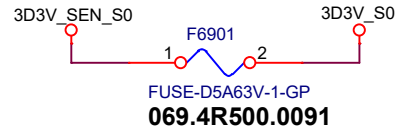


MP change to short pad



Main Func = Sensor (E-compass/A+Gyro/SAR)

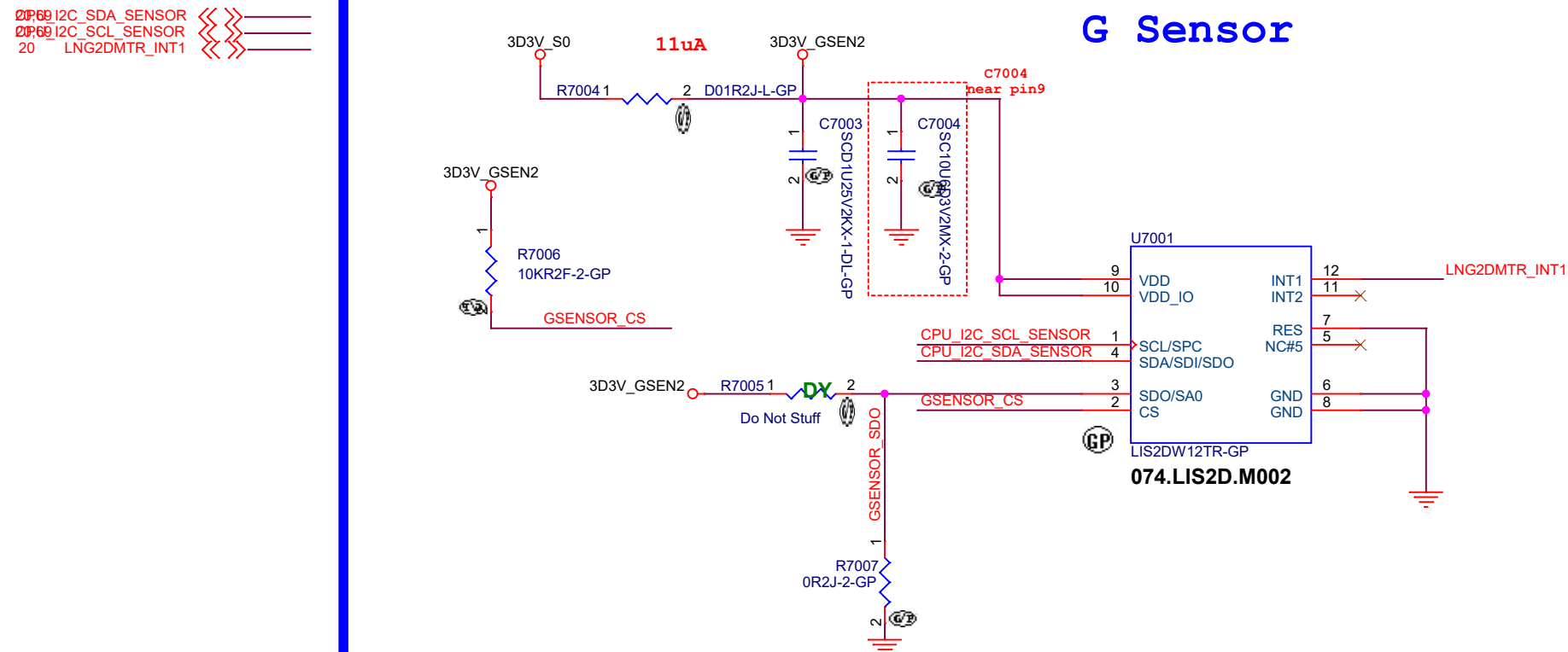
20 GSEN_INT1 <<< ———
CPU_I2C_SCL_SENSOR <<< ———
CPU_I2C_SDA_SENSOR <<< ———
USH_EXPANDER_SMBDAT <<< ———
USH_EXPANDER_SMBCLK <<< ———



Multi

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Title Sensor (GYROSCOPE/PRESSUE/ALS)			
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G Sensor



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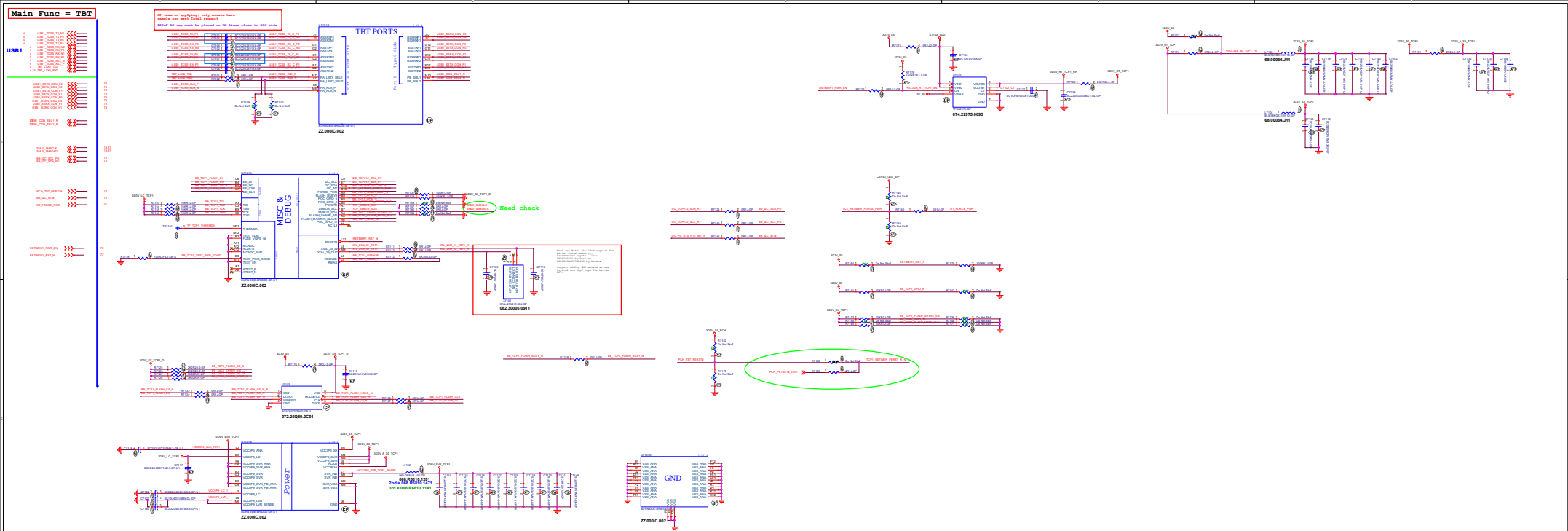
Sensor (G-sensor)

Document Number

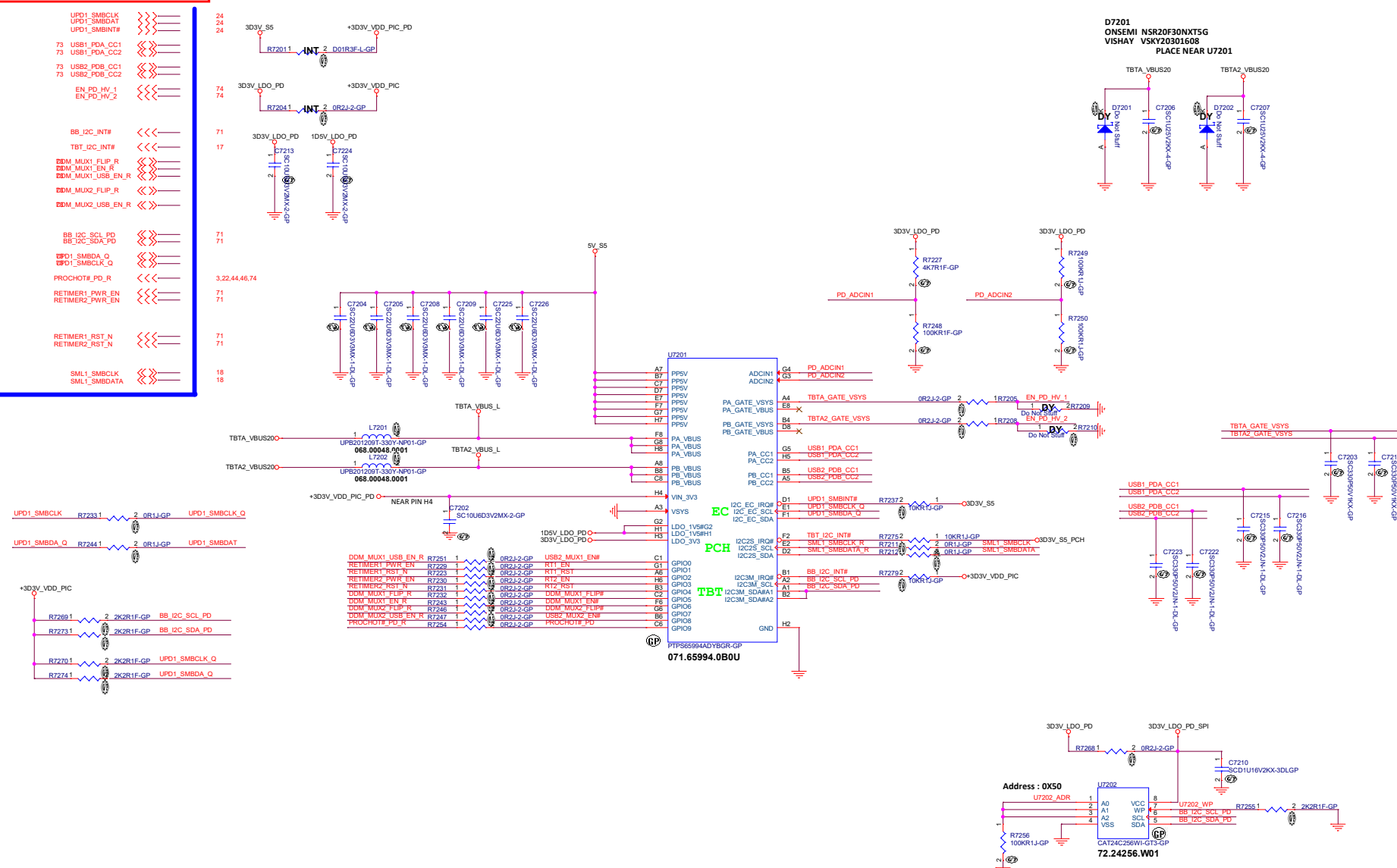
Rev
SB

Date: Friday, April 24, 2020

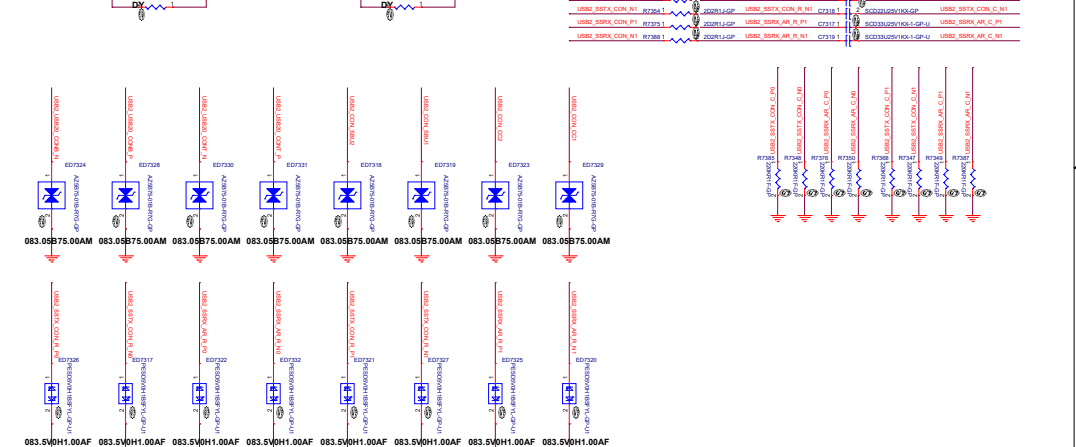
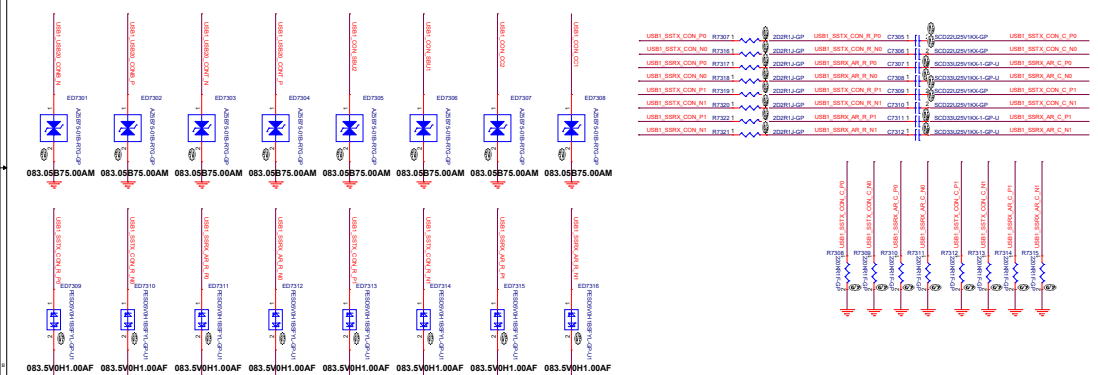
Sheet 70 of 106



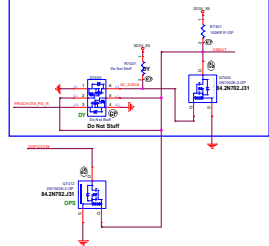
Main Func = TypeC



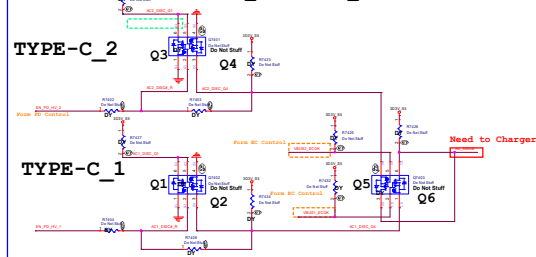
USB4



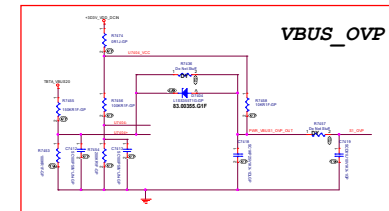
AC Disconnect Latch



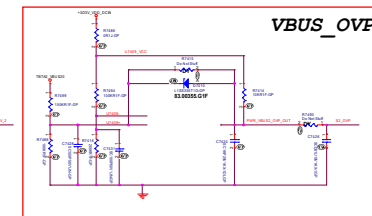
AC_Disconnect_Logic



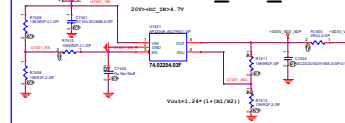
VBUS_OVP



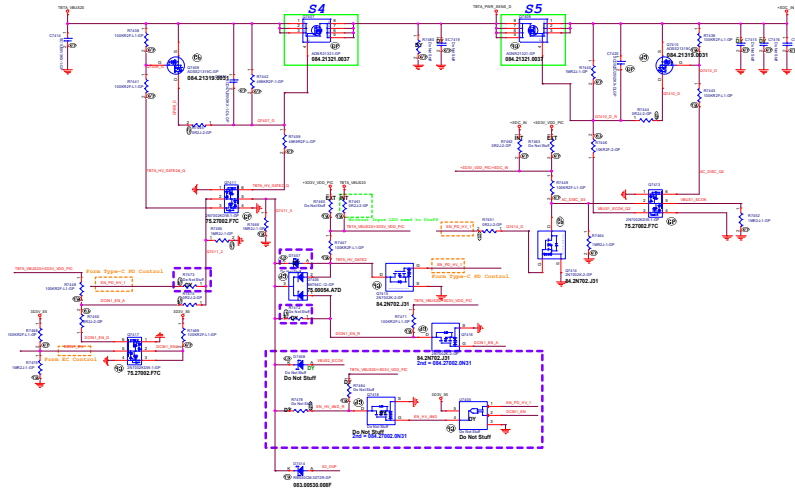
VBUS_OVP



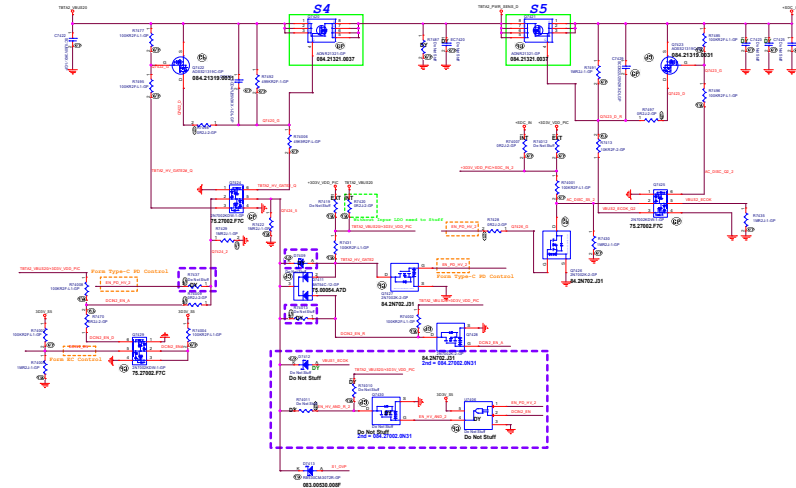
+3D3V_VDD_DCIN



TYPE-C 1




TYPE-C 2

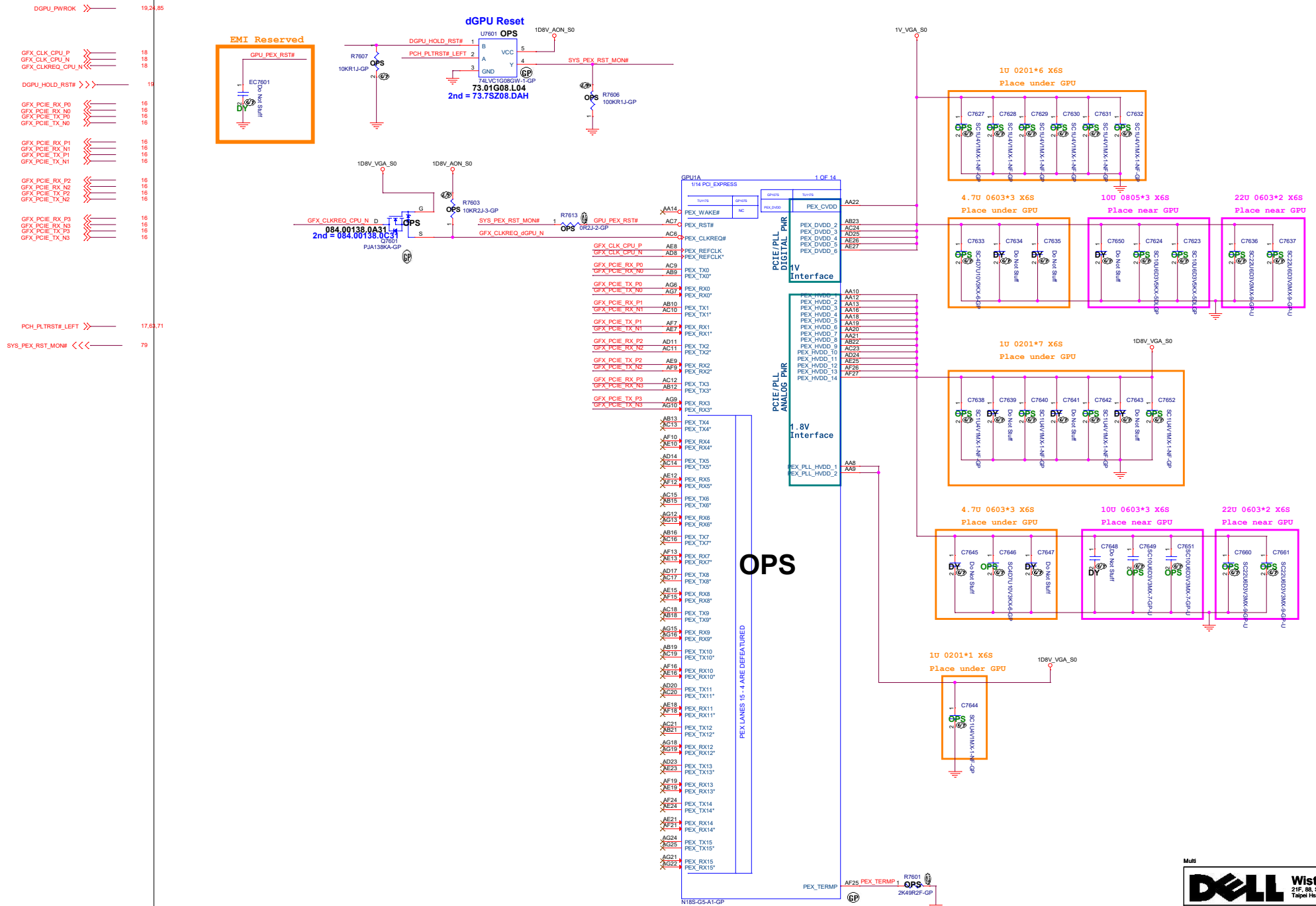


5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

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Title EXT IO (RSVD)			
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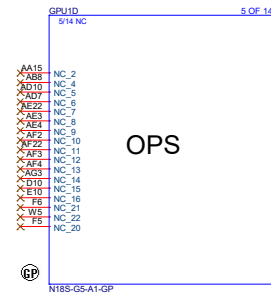
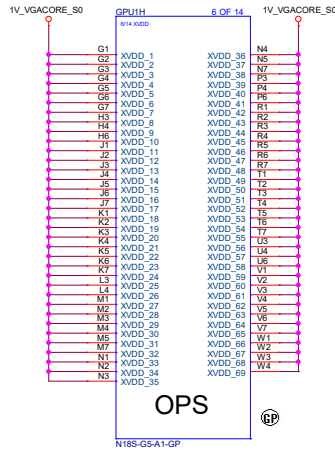
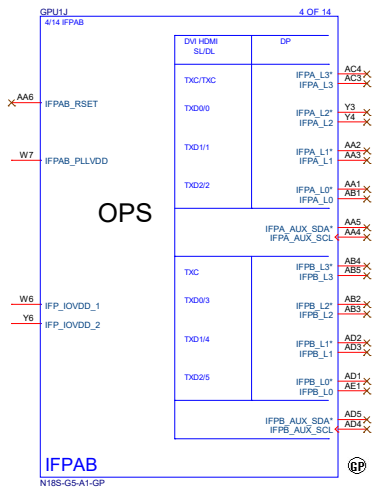
► PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 k Ω pull-up to 1V8_AON.



Multi



Main Func = dGPU



Multi

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File					
GPU DIGITALOUT (2/5)					
Size	Document Number	Rev			
A2	SouthPeak15 TGL	SB			
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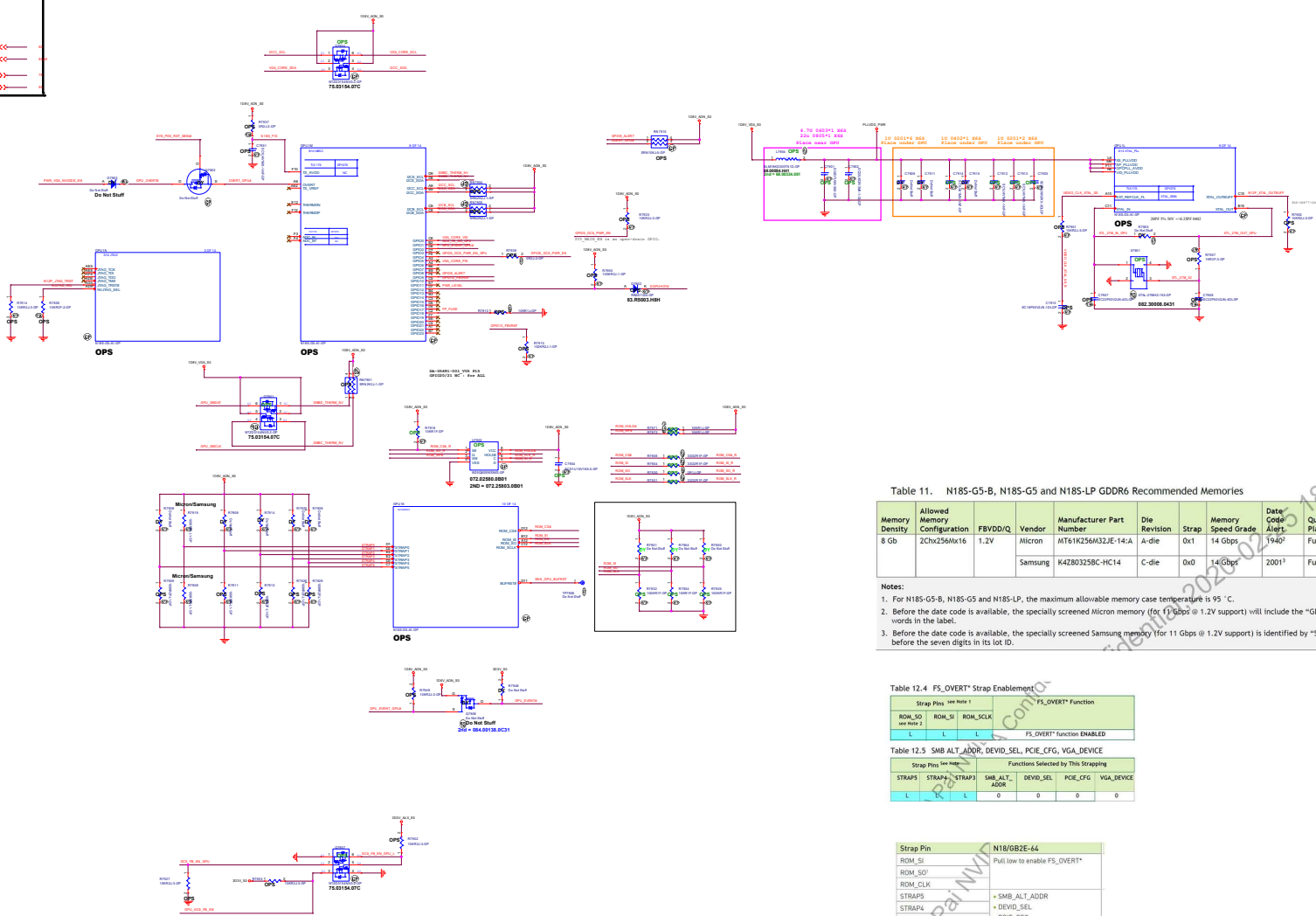
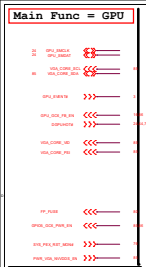


Table 11. N185-G5-B, N185-G5 and N185-LP GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256nx16	1.2V	Micron	MT61K256M32JE-14-A	A-die	0x1	14 Gbps	1940 ²	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 ³	Full	Production candidate

Notes:

- For N185-G5-B, N185-G5 and N185-LP, the maximum allowable memory case temperature is 95 °C.
- Before the date code is available, the specially screened Micron memory (for 11 Gbps @ 1.2V support) will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
- Before the date code is available, the specially screened Samsung memory (for 11 Gbps @ 1.2V support) is identified by "SPL" letters inserted before the seven digits in its lot ID.

Table 12.4 FS_OVERT* Strap Enablement

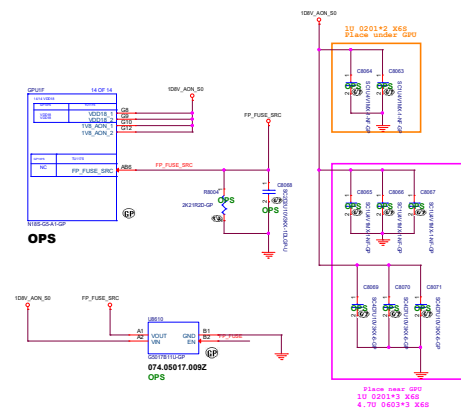
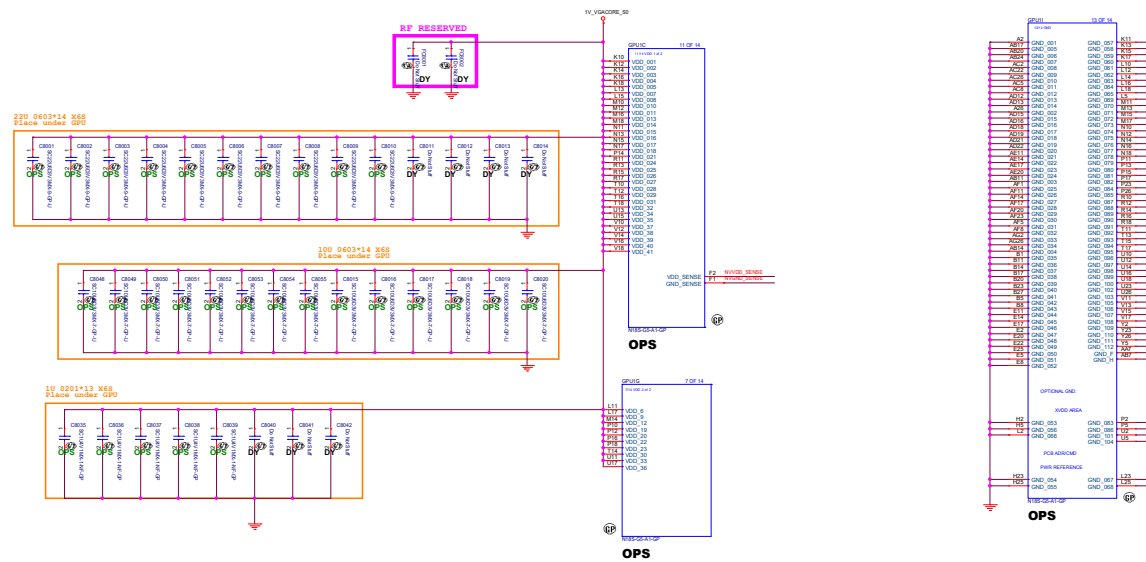
Strap Pins	FS_OVERT* Function
ROM_S0, ROM_S1, ROM_SCLK	FS_OVERT* Function ENABLED
L, L, L	FS_OVERT* Function DISABLED

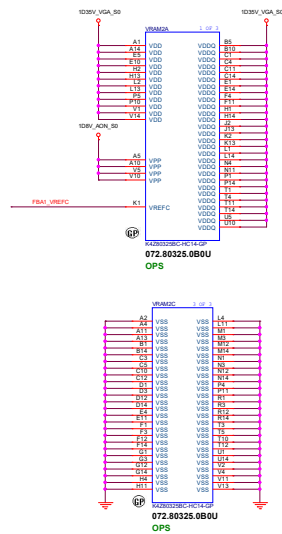
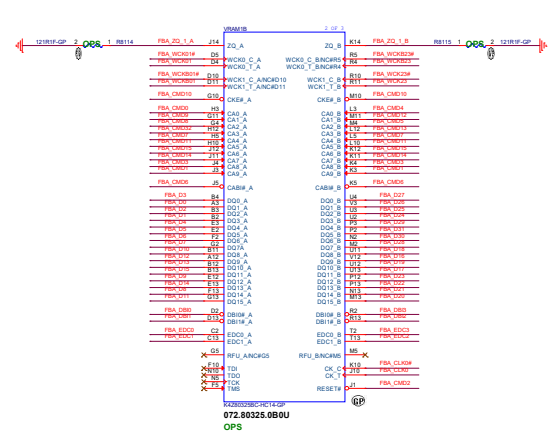
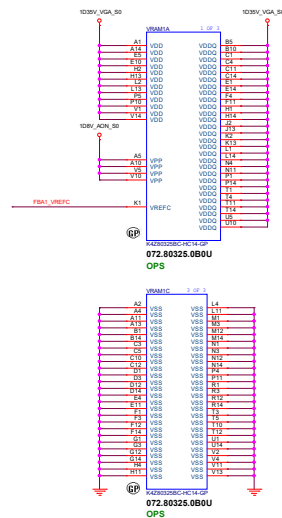
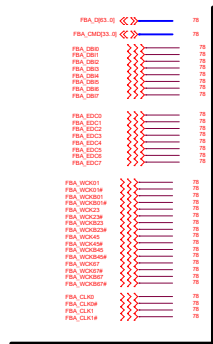
Table 12.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

STRAPS	STRAP3	STRAP2	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Strap Pin	N18/0B2E-44
ROM_S0	Pull low to enable FS_OVERT*
ROM_S1	
ROM_SCLK	
STRAP5	+ SMB_ALT_ADDR
STRAP4	+ DEVID_SEL
STRAP3	+ PCIE_CFG
STRAP2	+ VGA_DEVICE
STRAP1	RAMCFG6[6]
STRAP0	

Note:
The ROM_S0 pin should be pulled low using a 10 kΩ resistor for N18/0B2E-44 GPUs and using a 100 kΩ resistor for N17/0B2D-44/0B2C-44 GPUs.





8.2.2.14 GDDR6 DRAM VREFC
GDDR6 DRAMs include an integrated VREFC (VREF for DQ07 and ADDR). Figure 8-8 illustrates use of the integrated VREFC for x16 mode GDDR6 DRAM. Refer to the reference schematics for final component values.

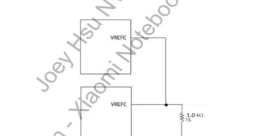
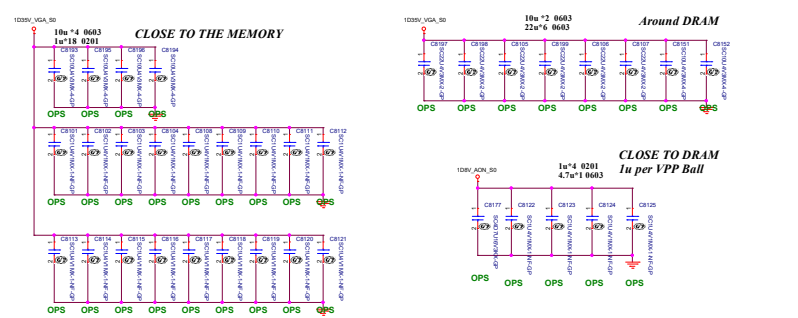


Figure 8-8 Use of Integrated VREFC for x16 Mode

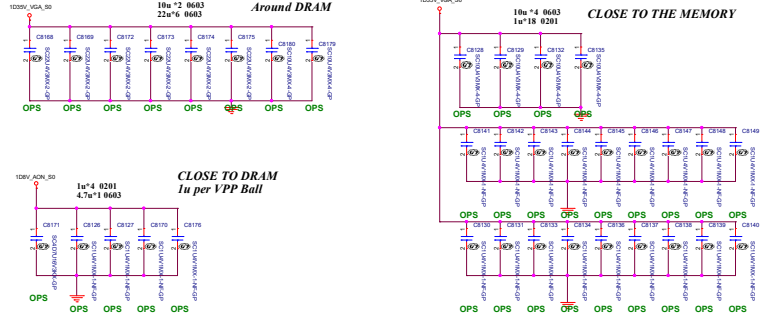
FOR VRAM1

PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE




FOR VRAM2

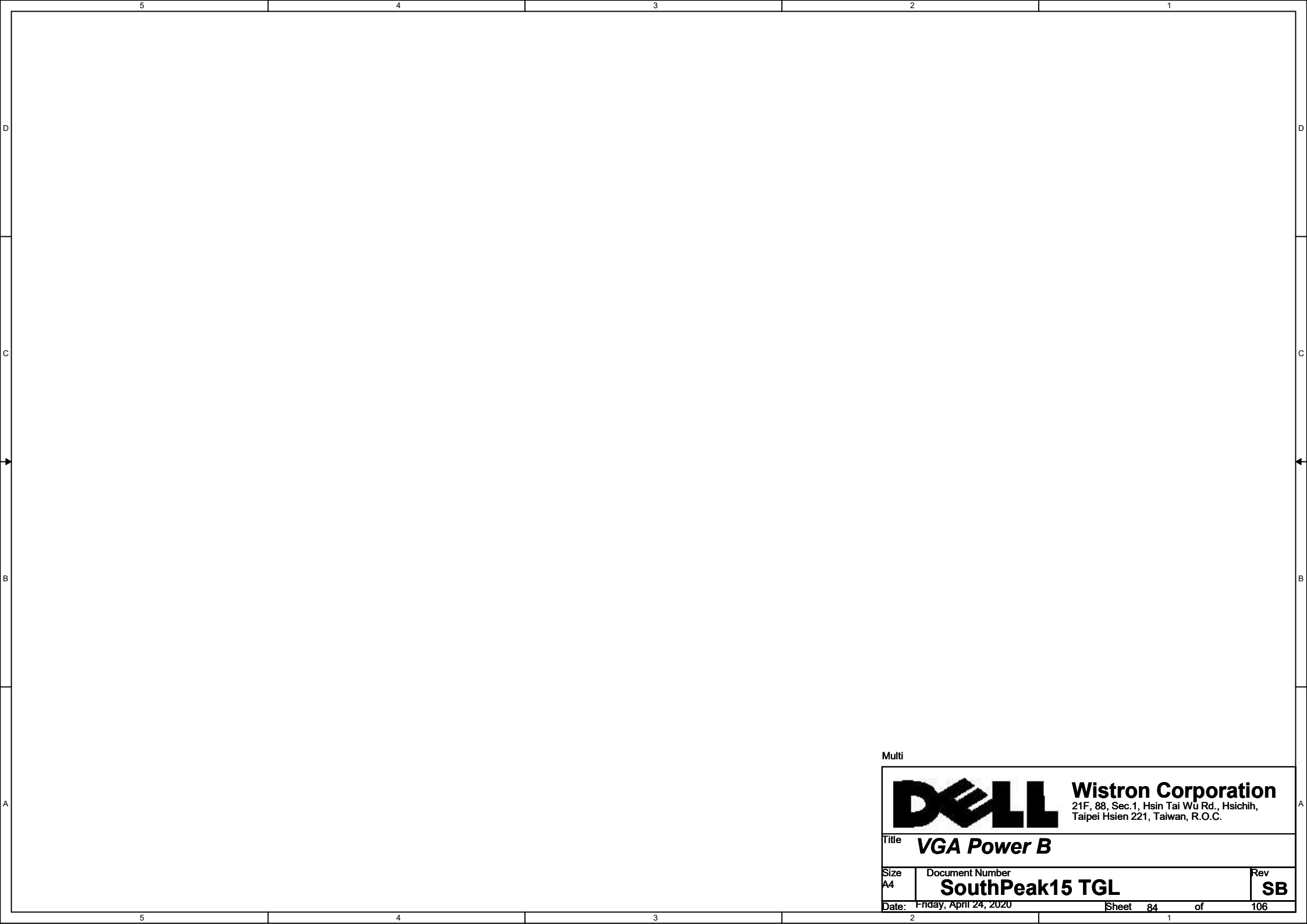
PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE




5	4	3	2	1
D				
C				
B				
A				

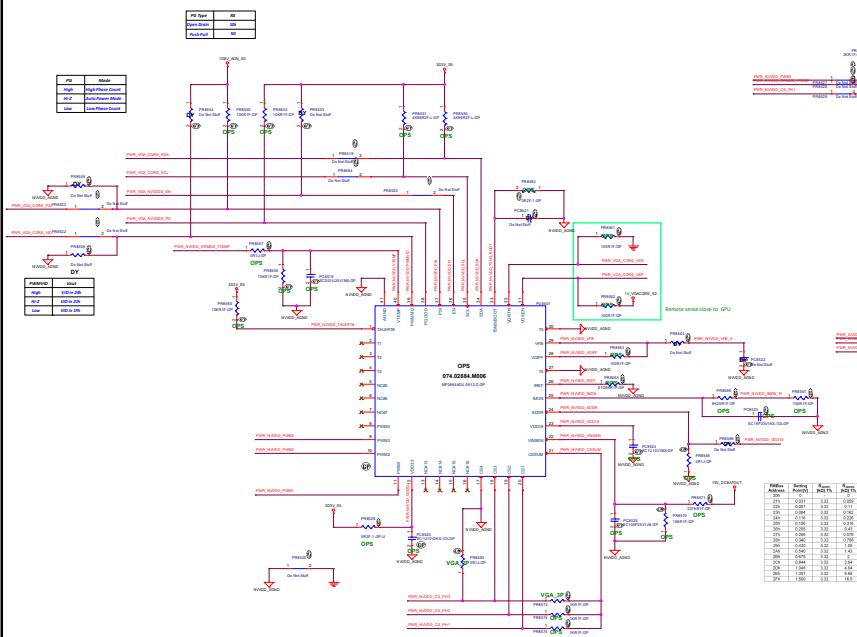
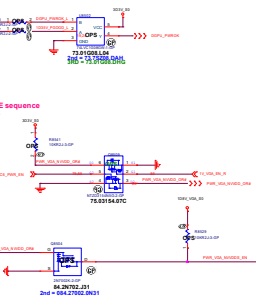
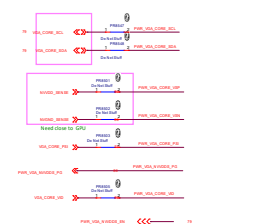
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title VGA Power A			
Size A4	Document Number SouthPeak15 TGL		Rev SB
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Title VGA Power B					
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Part	Value	Unit
PC8530	100	nF
PC8531	100	nF
PC8532	100	nF
PC8533	100	nF
PC8534	100	nF
PC8535	100	nF
PC8536	100	nF
PC8537	100	nF
PC8538	100	nF
PC8539	100	nF
PC8540	100	nF
PC8541	100	nF
PC8542	100	nF
PC8543	100	nF
PC8544	100	nF
PC8545	100	nF
PC8546	100	nF
PC8547	100	nF
PC8548	100	nF
PC8549	100	nF
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PC8551	100	nF
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PC8568	100	nF
PC8569	100	nF
PC8570	100	nF
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PC8594	100	nF
PC8595	100	nF
PC8596	100	nF
PC8597	100	nF
PC8598	100	nF
PC8599	100	nF
PC8600	100	nF

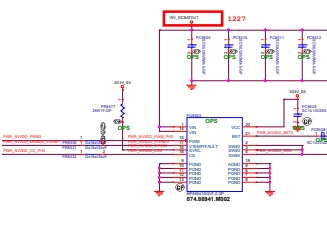
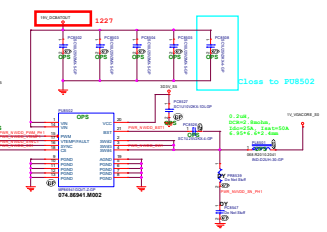
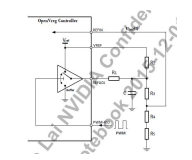
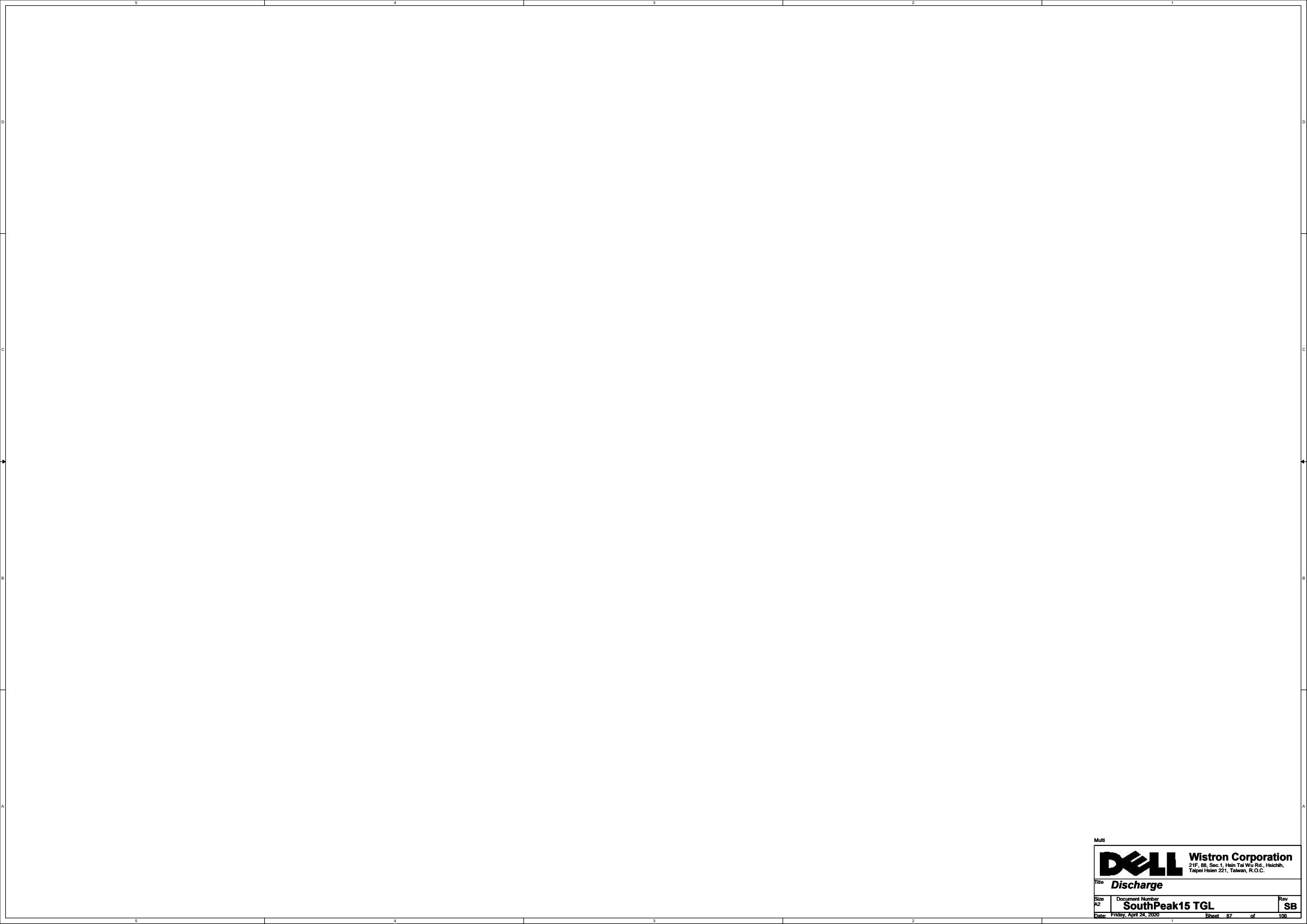


Table 7.8 PWM-VID Spec and Component Values		
PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	100
PWM Frequency F_{PWM}	kHz	6.25
PWM Minimum Pulse Width T_{min}	ns	5.26
VID Transient Time T	ns	>100
Component Value		
R1 (1%)	kΩ	6.19
R2 (1%)	kΩ	20.5
R3 (1%)	kΩ	4.32
R4 (1%)	kΩ	16.5
R5 (1%)	kΩ	8.20
C	μF	



Location	VGA_3P	VGA_2P
PC8530	Stuff	DY
PC8531	Stuff	DY
PC8532	Stuff	DY
PC8533	Stuff	DY
PC8534	Stuff	DY
PC8535	Stuff	DY
PC8536	Stuff	DY
PC8537	Stuff	DY
PC8538	Stuff	DY
PC8539	Stuff	DY
PC8540	Stuff	DY
PC8541	Stuff	DY
PC8542	Stuff	DY
PC8543	Stuff	DY
PC8544	Stuff	DY
PC8545	Stuff	DY
PC8546	Stuff	DY
PC8547	Stuff	DY
PC8548	Stuff	DY
PC8549	Stuff	DY
PC8550	Stuff	DY
PC8551	Stuff	DY
PC8552	Stuff	DY
PC8553	Stuff	DY
PC8554	Stuff	DY
PC8555	Stuff	DY
PC8556	Stuff	DY
PC8557	Stuff	DY
PC8558	Stuff	DY
PC8559	Stuff	DY
PC8560	Stuff	DY
PC8561	Stuff	DY
PC8562	Stuff	DY
PC8563	Stuff	DY
PC8564	Stuff	DY
PC8565	Stuff	DY
PC8566	Stuff	DY
PC8567	Stuff	DY
PC8568	Stuff	DY
PC8569	Stuff	DY
PC8570	Stuff	DY
PC8571	Stuff	DY
PC8572	Stuff	DY
PC8573	Stuff	DY
PC8574	Stuff	DY
PC8575	Stuff	DY
PC8576	Stuff	DY
PC8577	Stuff	DY
PC8578	Stuff	DY
PC8579	Stuff	DY
PC8580	Stuff	DY
PC8581	Stuff	DY
PC8582	Stuff	DY
PC8583	DY	Stuff

Table 7.9 PWM-VID Spec and Component Values		
PWM-VID Specification		Config
V _{min}	V	0.3
V _{max}	V	1.3
V _{boot}	V	0.8
Voltage Step V _{step}	mV	6.25
Number of Voltage Levels N	Level	160
PWM Frequency F _{PWM}	kHz	5.76
PWM Minimum Pulse Width T _{min}	ns	5.26
VID Transient Time T	ns	200
Component Value		
R1 (1%)	kΩ	6.19
R2 (1%)	kΩ	20.5
R3 (1%)	kΩ	4.32
R4 (1%)	kΩ	16.5
R5 (1%)	kΩ	8.20
C	μF	1.5




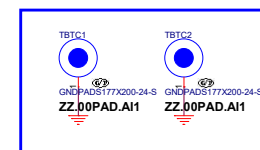
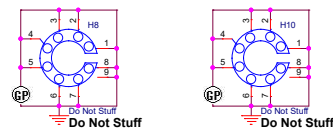
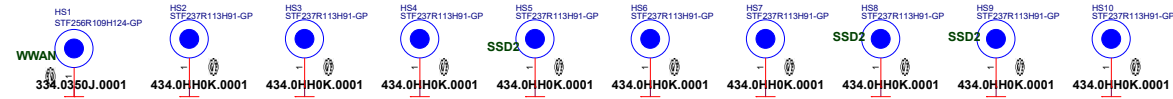
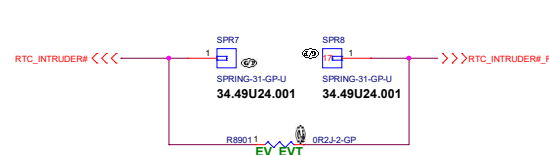
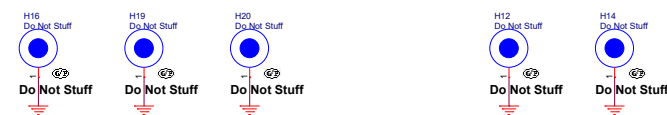
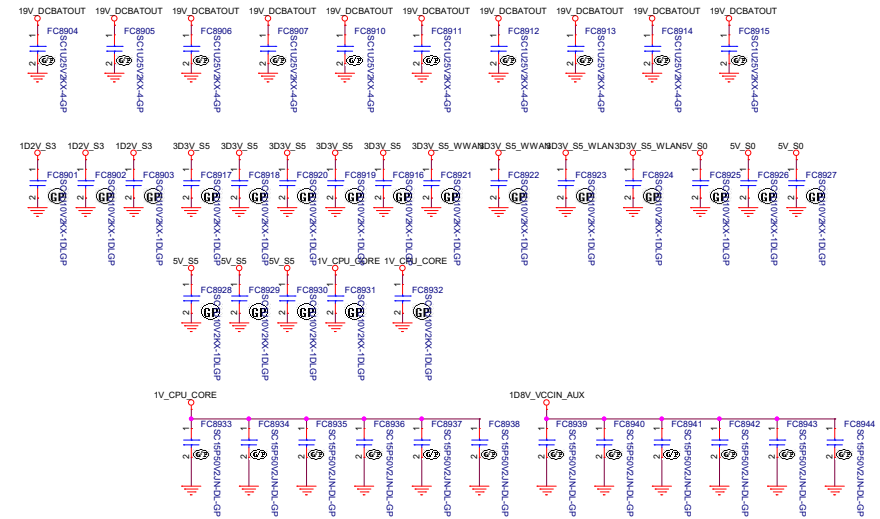
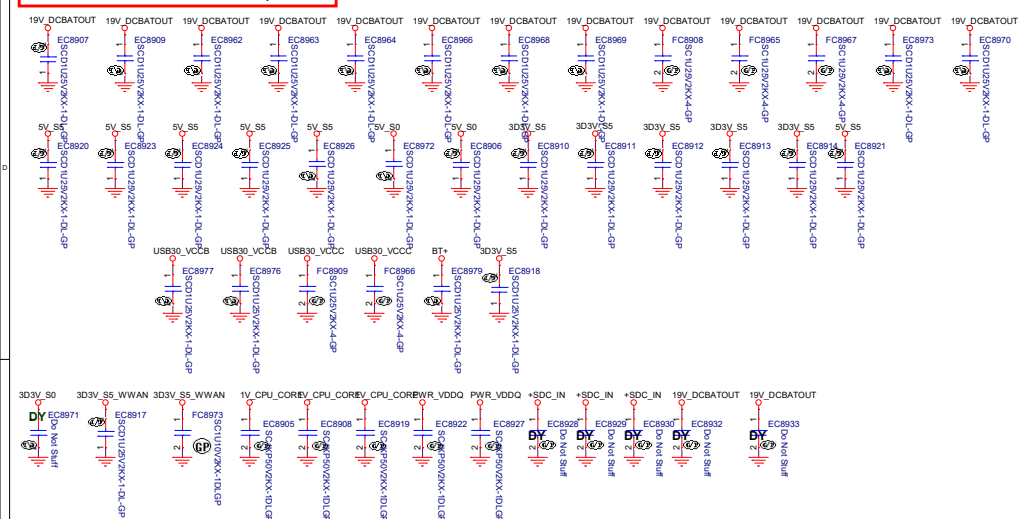
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Discharge			
Size A2	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 25, 2008 Sheet 87 of 108			

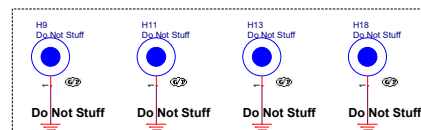
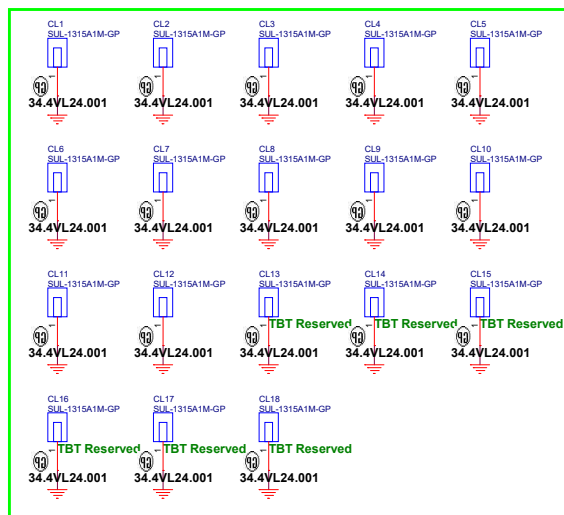
5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title UNUSED PARTS (RSVD)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 88 of	106

$$\text{Main Func} = \text{EMC} / \text{RF}$$



TBT XTAL shielding can
434.0M601.0001



Lavout need

5	4	3	2	1
D				
C				
B				
A				

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD) (NFC)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 90 of	106

Main Func = TPM

```

TPM_PIRQ#
SIO_SLP_S0#
PCH_PLTRST#_RIGHT

```

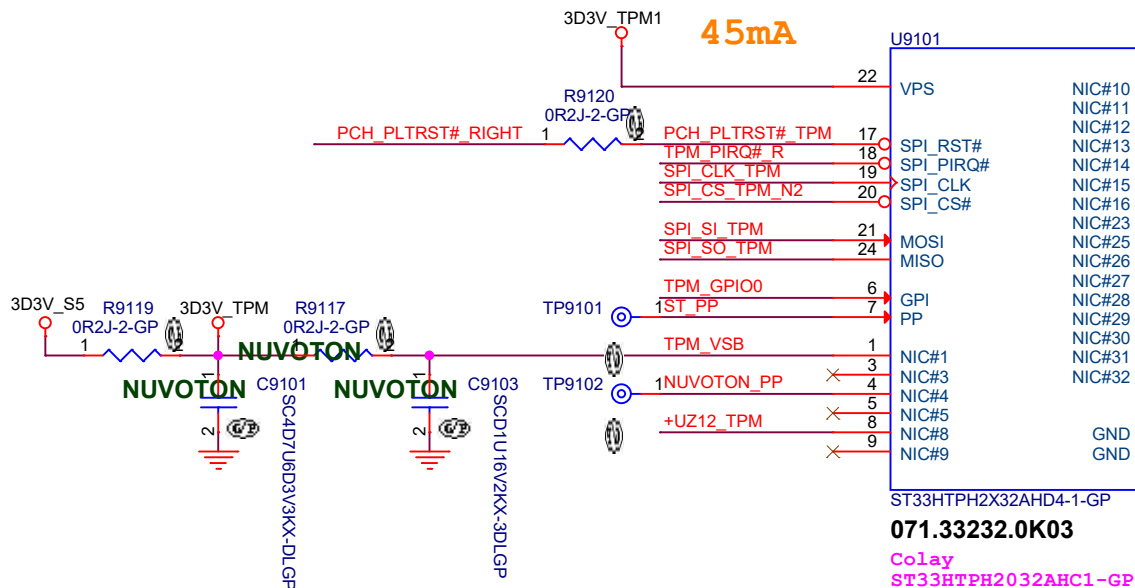
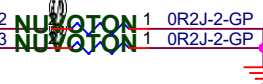
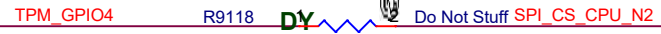
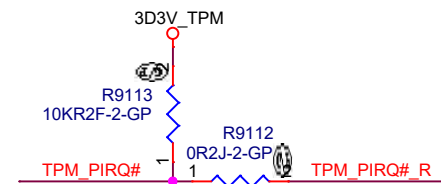
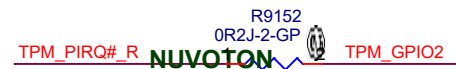
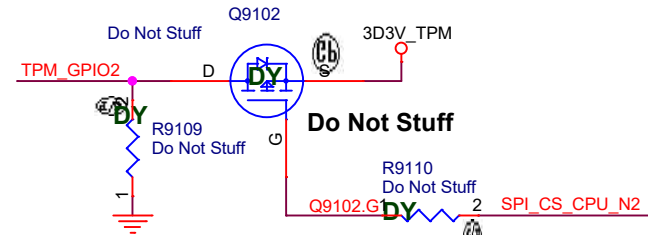
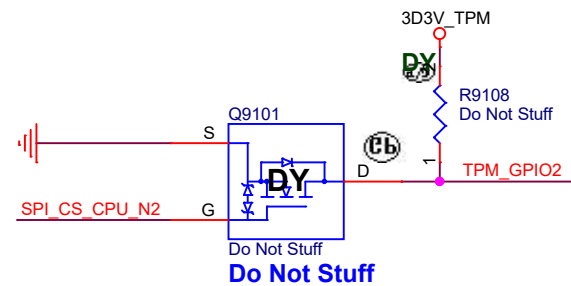
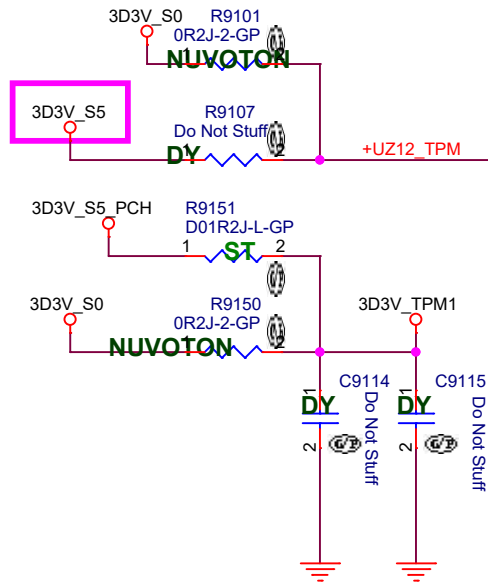
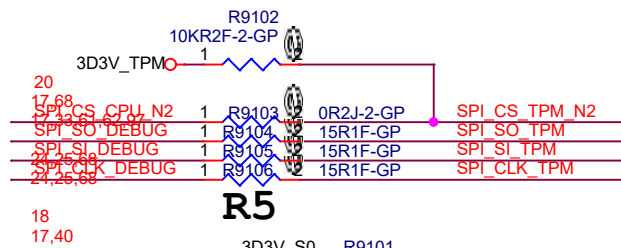
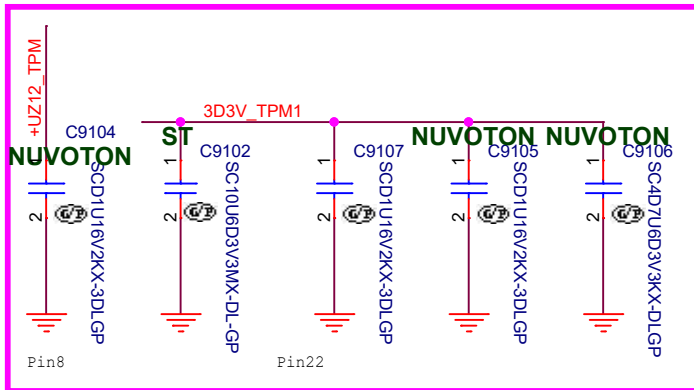
24,25,68

SPI_CLK_DEBUG	~	~	~	~
SPI_SI_DEBUG	~	~	~	~
SPI_SO_DEBUG	~	~	~	~
SPI_CS_CPU_N2	~	~	~	~
CPU_C10_GATE#	~	~	~	~

```

96     SPI_CLK_TPM    <<<=====
96     SPI_SI_TPM     <<<=====

```



ST33HTPH2X32AHD4-1-GP

071.33232.0K03

Colay

ST33HTPH2032AH0
071.33232.0K03

NPCT750JAAYX-1-GP

071.00750.M001



Wistron Corporation

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Title

INT 10 (TPM)

Size

Document Number

Rev

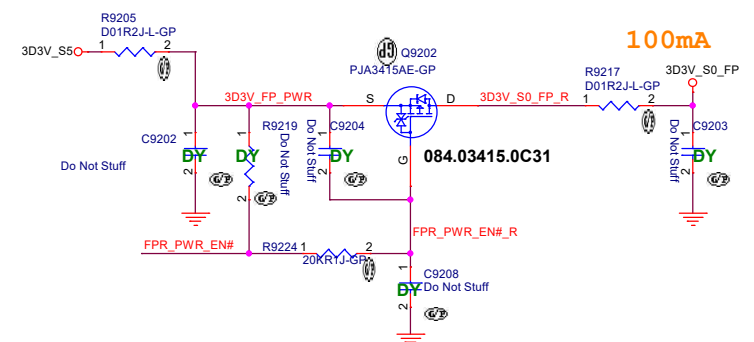
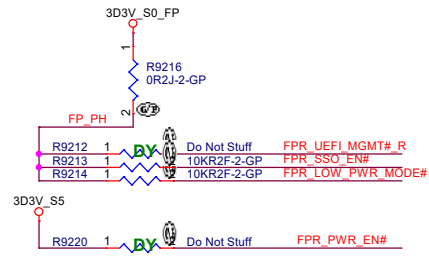
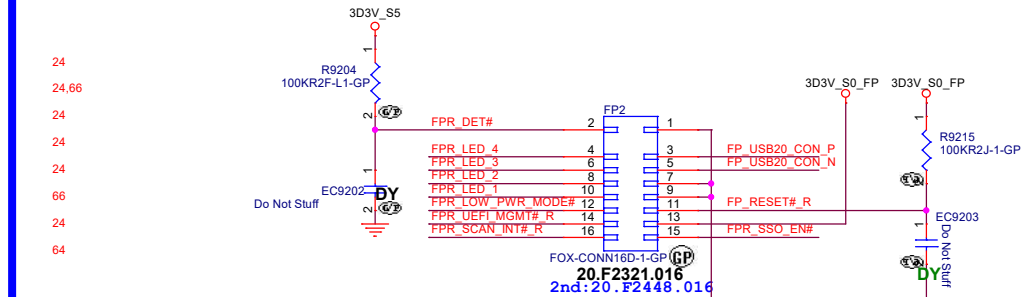
SB

Date: Friday, April 24, 2020

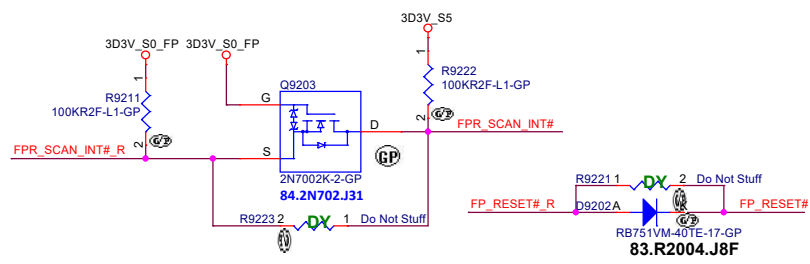
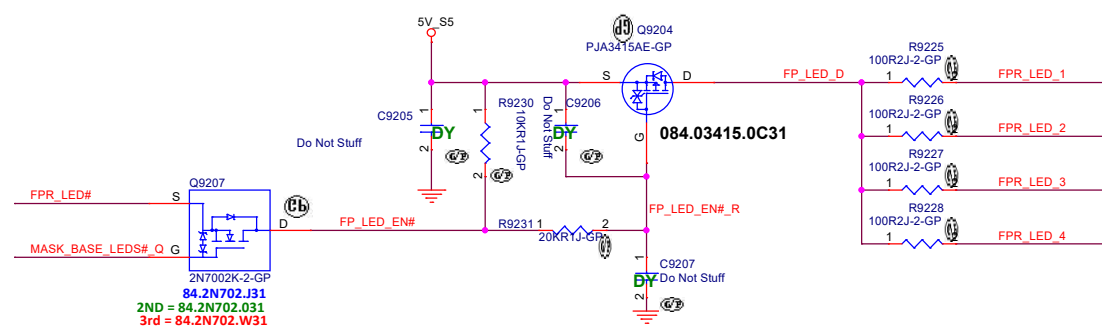
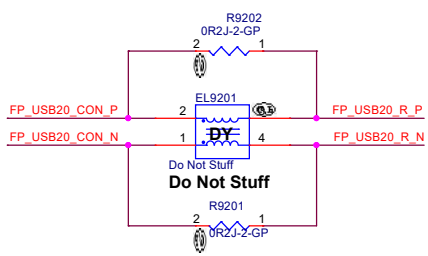
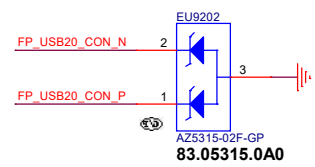
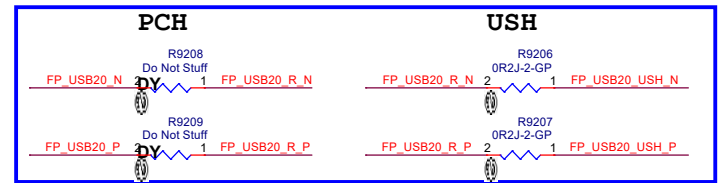
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Main Func = Finger Printer

FP_USB20_P	<<>>	
FP_USB20_N	<<>>	
FPR_DET#	<<<<	24,64
FP_USB20_USH_N	<<>>	
FP_USB20_USH_P	<<>>	
FPR_PWR_EN#	>>>>	24
FPR_SCAN_INT#	<<<<	24,66
FPR_SSO_EN#	>>>>	24
FPR_UEFI_MGMT#_R	>>>>	24
FPR_LOW_PWR_MODE#	>>>>	24
FP_RESET#	>>>>	66
FPR_LED#	>>>>	24
MASK_BASE_LEDS#_Q	>>>>	64



Try to co-lay



Multi

DELL Wistron Corporation
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Title: **INT IO (Finger Printer)**

Size: A3 Document Number: Rev: SB

Date: Friday, April 24, 2020 Sheet: 92 of 106


5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (RSVD) (Express Card/PCIE slot)		
Size A4	Document Number	Rev SB
Date: Friday, April 24, 2020		Sheet 93 of 106


5	4	3	2	1
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C				C
B				B
A				A

Multi

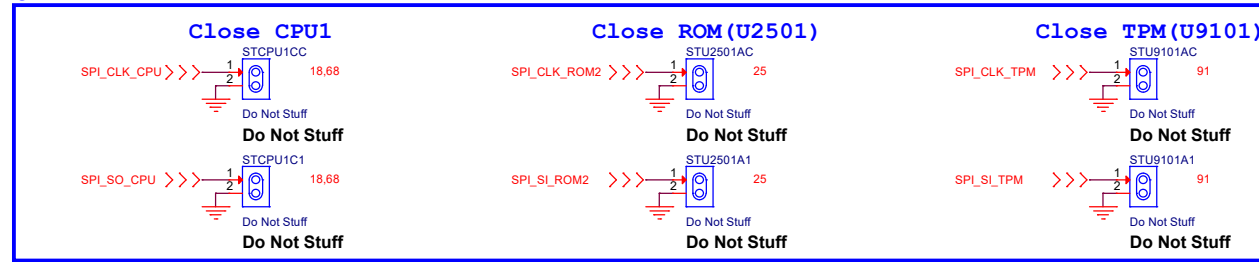
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (RSVD) (Smart Card/COM/PS2)		
Size A4	Document Number	Rev SB
Date: Friday, April 24, 2020		Sheet 94 of 106

5	4	3	2	1
D				D
C				C
B				B
A				A

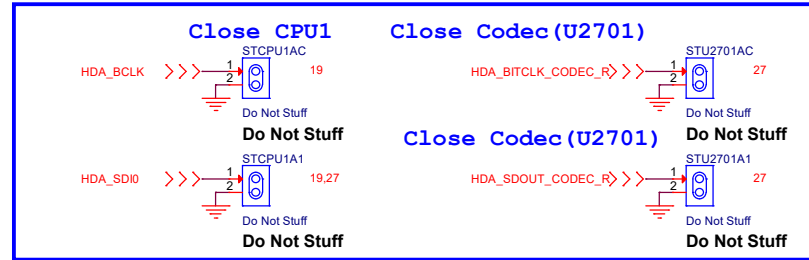
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title EXT IO (RSVD) (Docking/LPT)			
Size A4	Document Number		Rev SB
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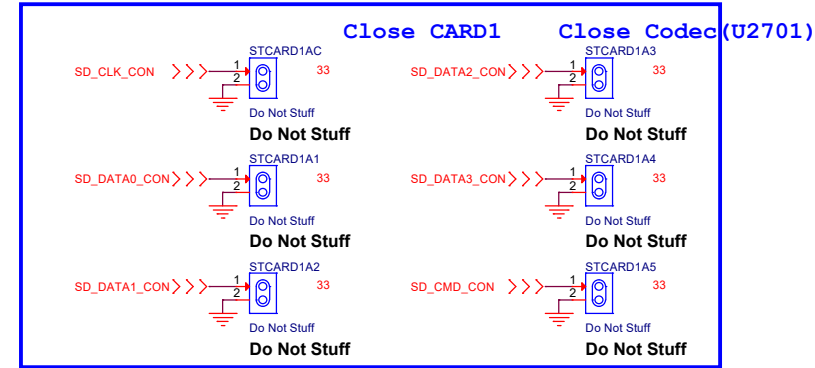
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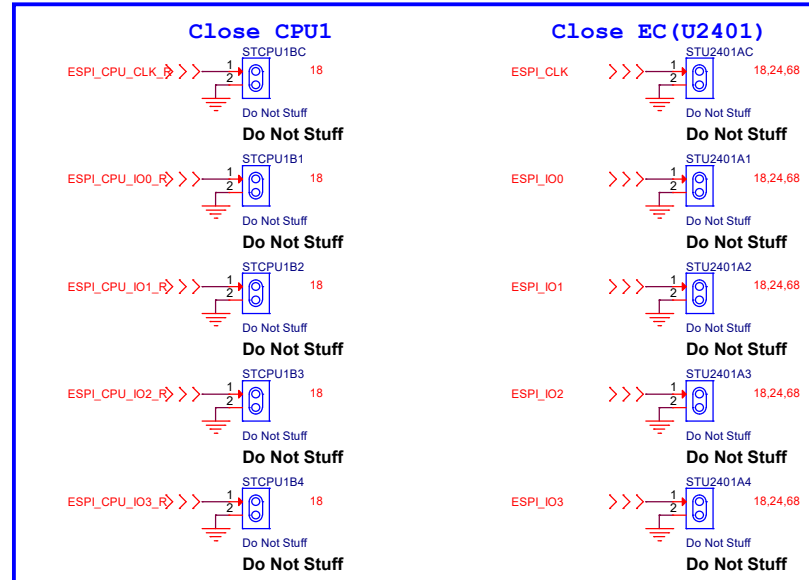
HDA



SDIO



ESPI



Multi

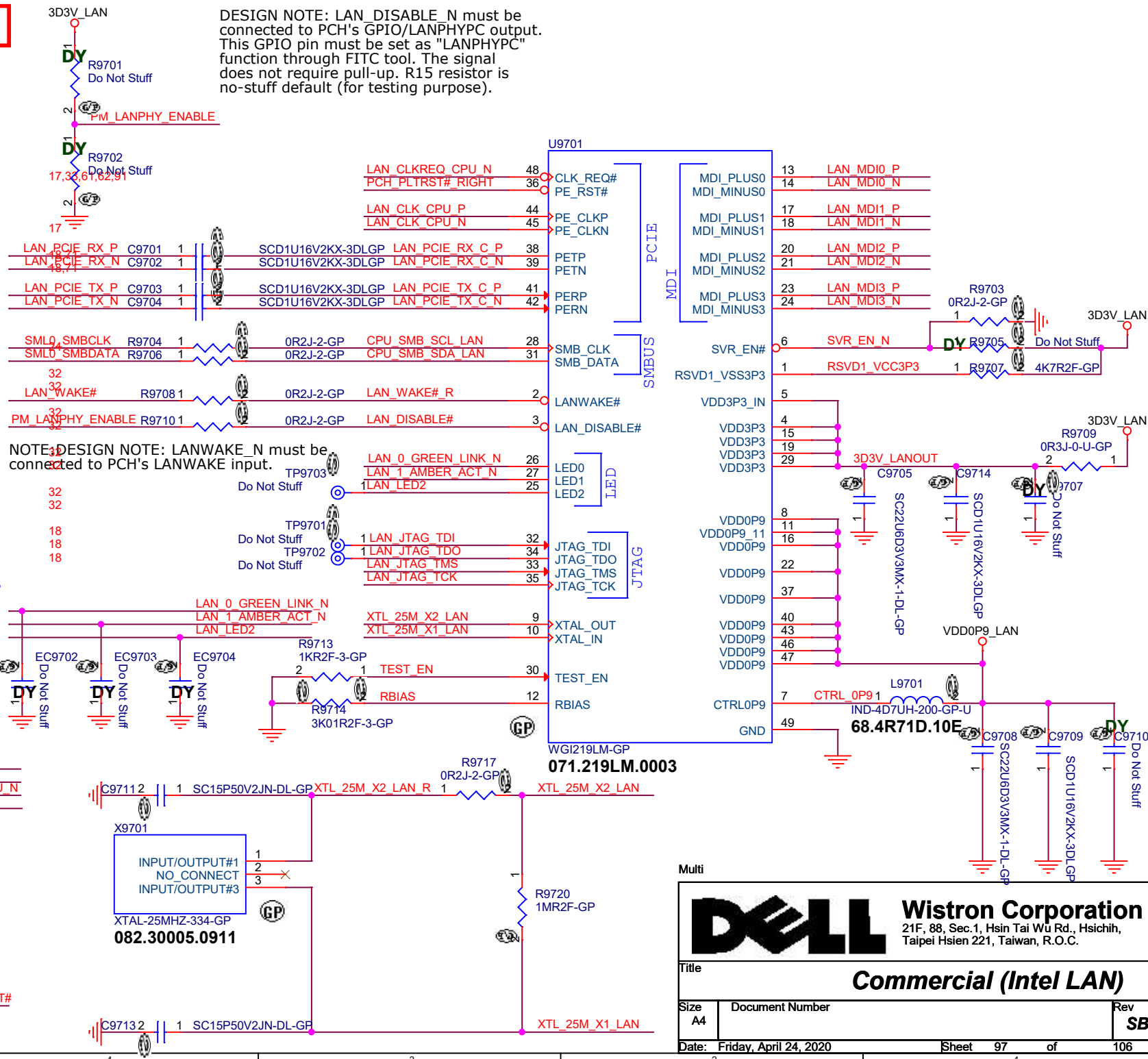
Main Func = LAN

LAN


16LAN_PCIE_RX_N
16LAN_PCIE_RX_P
16LAN_PCIE_TX_N
16LAN_PCIE_TX_P

PCH_PLTRST#_RIGHT >>>
17 LAN_WAKE# <<<
PM_LANPHY_ENABLE >>>
SML0_SMBCLK <<<
SML0_SMBDATA <<<
32 LAN_0_GREEN_LINK_N <<<
32 LAN_1_AMBER_ACT_N <<<
LOM_CABLE_DETECT# <<
LAN_MDIO_P >>>
LAN_MDIO_N >>>
LAN_MDIO1_P >>>
LAN_MDIO1_N >>>
LAN_MDIO2_P >>>
LAN_MDIO2_N >>>
LAN_MDIO3_P >>>
LAN_MDIO3_N >>>
LAN_CLK_CPU_N <<<
LAN_CLK_CPU_P <<<
LAN_CLKREQ_CPU_N <<<

DESIGN NOTE: LAN_DISABLE_N must be connected to PCH's GPIO/LANPHYPC output. This GPIO pin must be set as "LANPHYPC" function through FITC tool. The signal does not require pull-up. R15 resistor is no-stuff default (for testing purpose).



Multi



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Title

Commercial (Intel LAN)

Size
A4

Document Number

Rev
SB

Date
Friday, April 24, 2020

Sheet
97

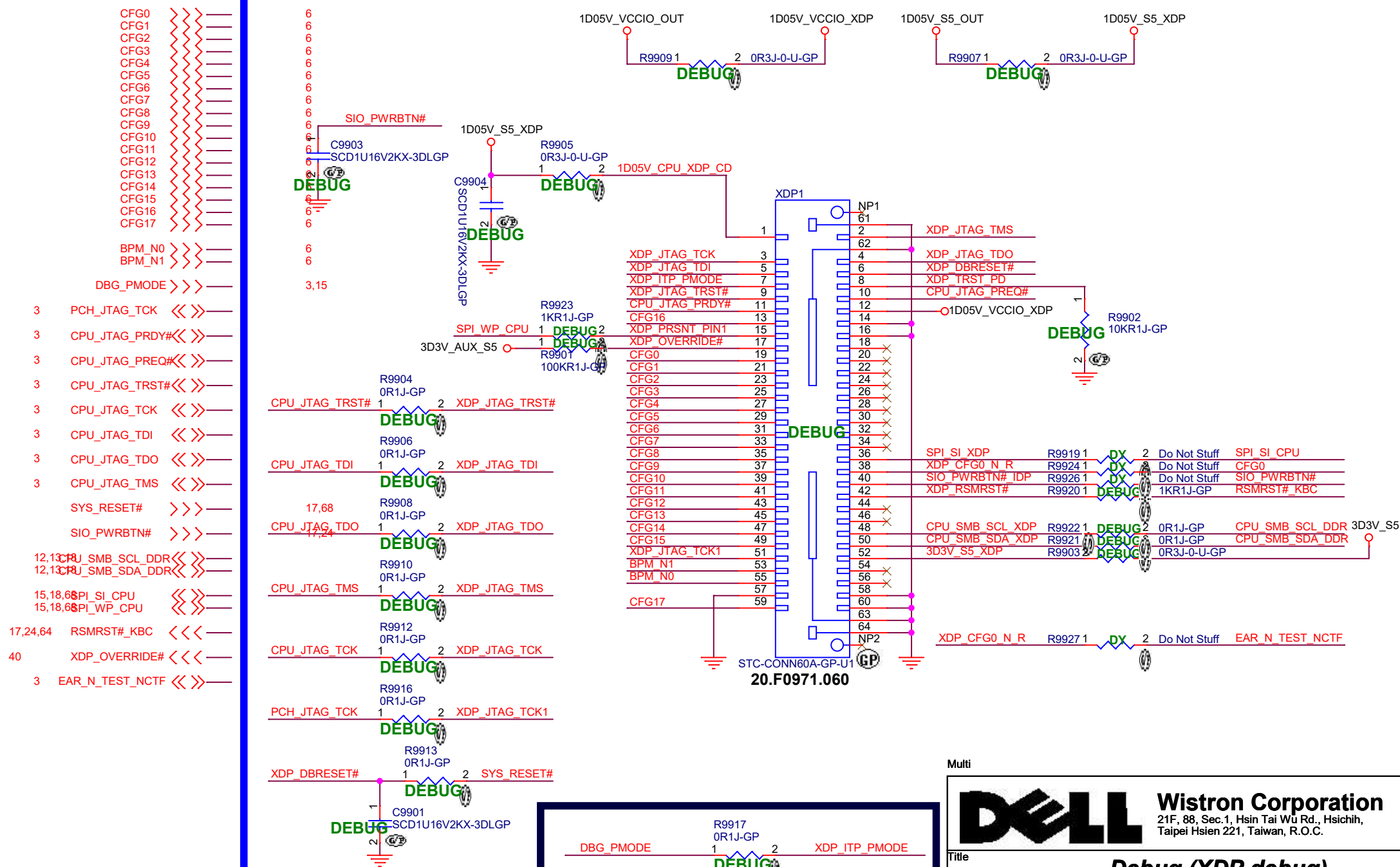
of
106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Commercial (LAN Switch)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 98 of	106

Main Func = Debug (MIPI)



Pull high on Page15



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Title

Debug (XDP debug)

Size

Document Number

SouthPeak15 TGL

Rev

SE

Date: Friday, April 24, 2020

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Table of Content

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603


The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,.....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceramic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

Multi



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 Taipei Hsien 221, Taiwan, R.O.C.

Title

Table of Content

Size

A4

Document Number

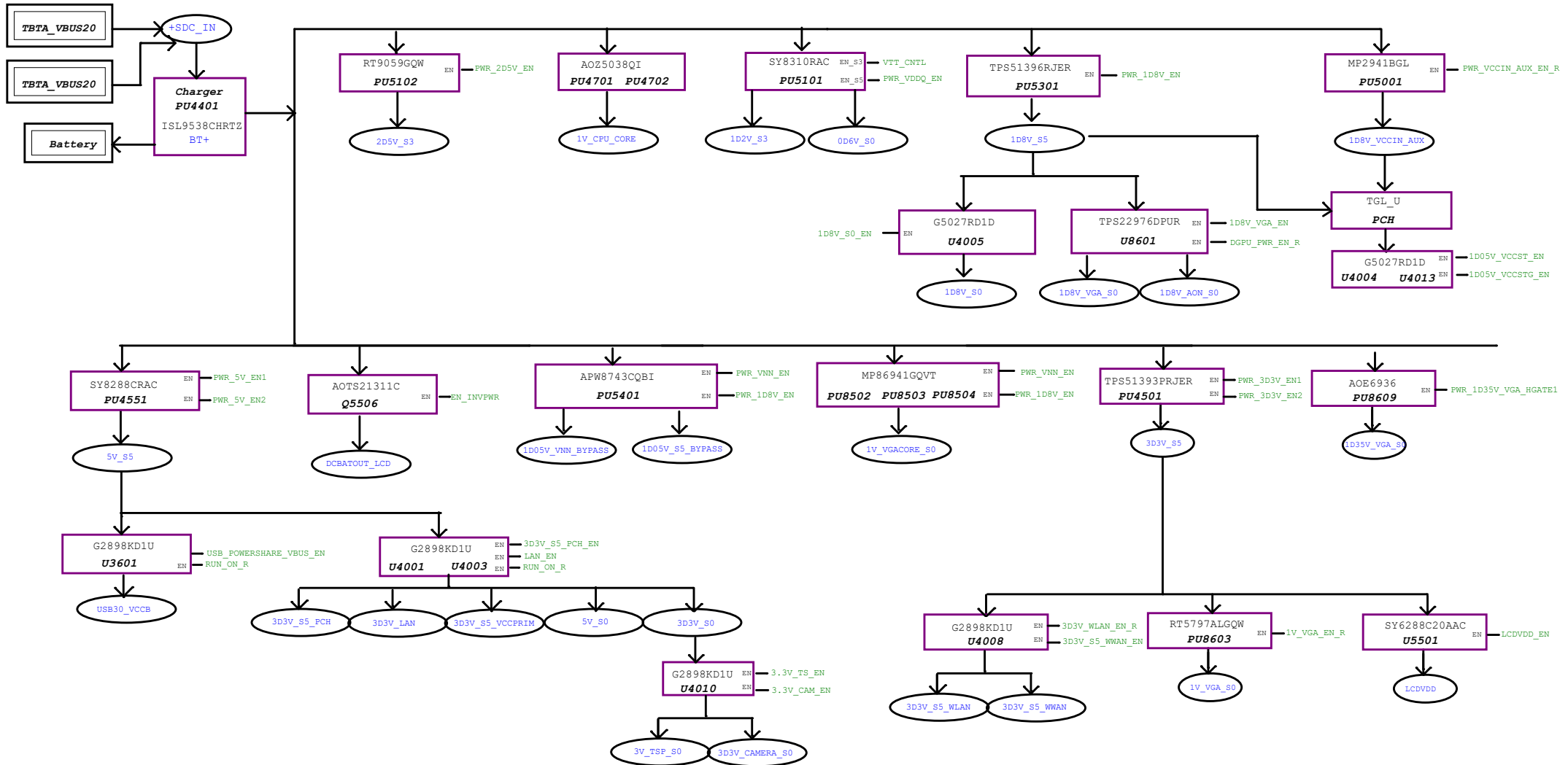
Rev

SB

Date: Friday, April 24, 2020

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Multi

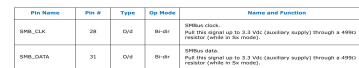
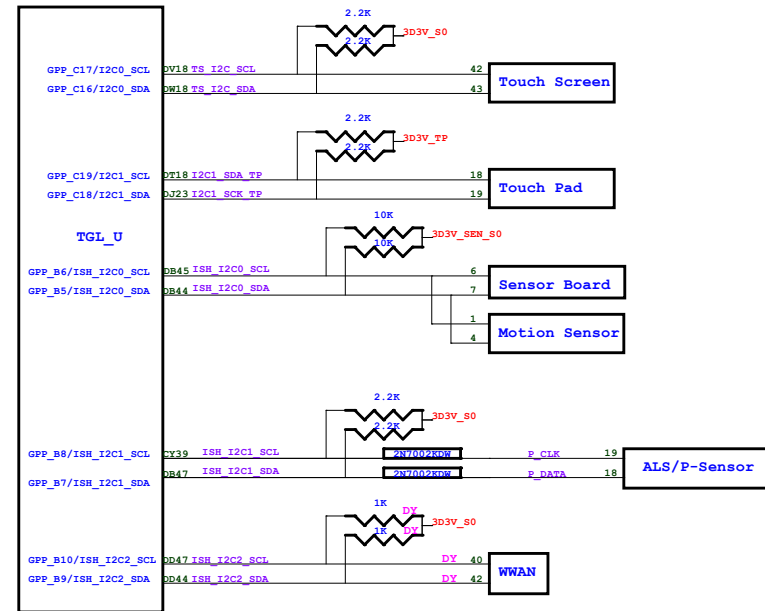


Title **Power Block Diagram**

Size A2 Document Number Rev SB

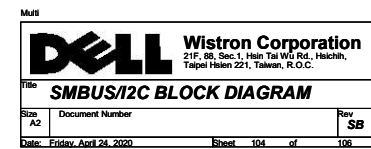
Date: Friday, April 24, 2020 Sheet 103 of 106

I2C Block Diagram

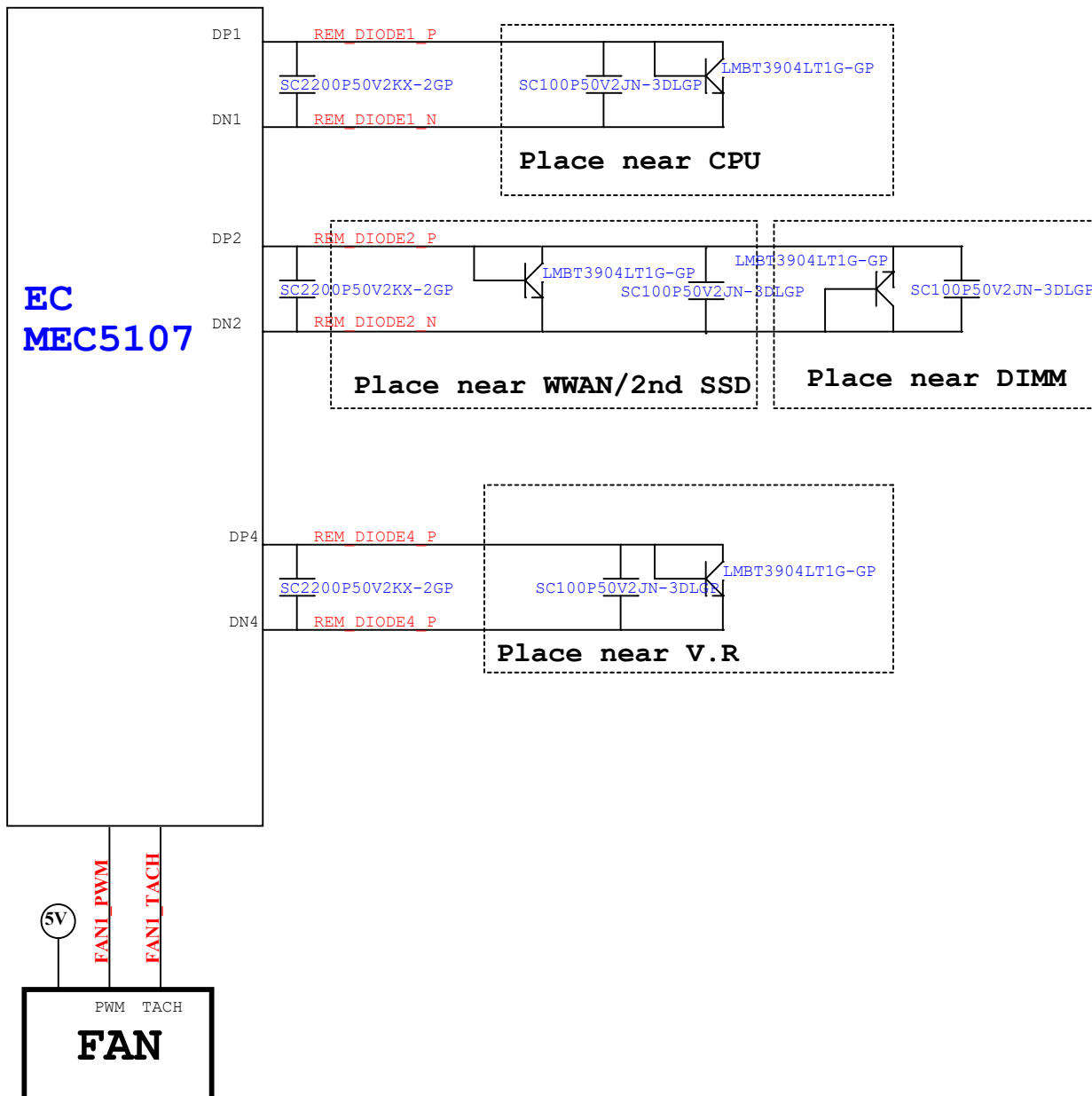


Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance (C_b)	External Pull-up	PCH Pull Down Strength (Refer EDS)
Up to 400 pF	2.2KΩ	100Ω
Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings		
Total Bus Capacitance (C_b)	External Pull-up	PCH Pull Down Strength

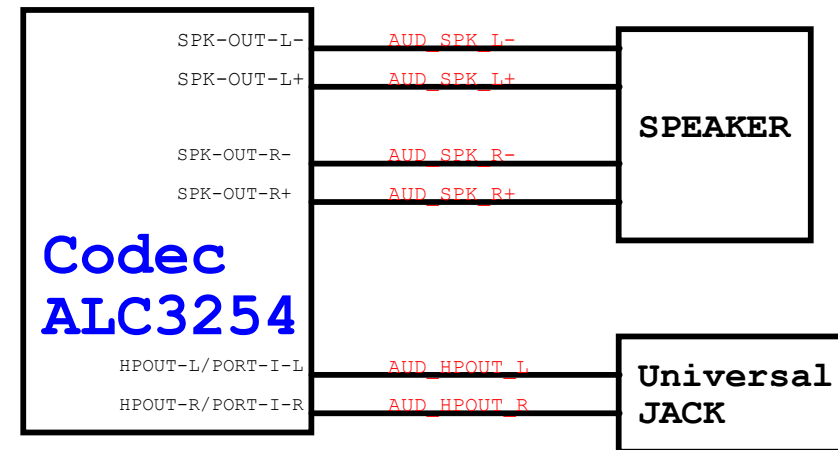
	Up to 100pF	2.7KΩ	1000
	Up to 200pF	1.5KΩ	
	Up to 300pF	1KΩ	
	Up to 400 pF	680Ω	
Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings			
Total Bus Capacitance (C_B)	External Pull-up		PCH Pull Down Strength
Up to 50pF	2.2KΩ		100Ω
Up to 100pF	1.2KΩ		
Up to 200pF	560Ω		
Up to 300pF	390Ω		
Up to 400 pF	270Ω		67Ω



Thermal Block Diagram



Audio Block Diagram




Multi

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title THERMAL/AUDIO BLOCK DIAGRAM			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 105 of	106

5	4	3	2	1
D				
C				
B				
A				

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CLK Block			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 106	of 106